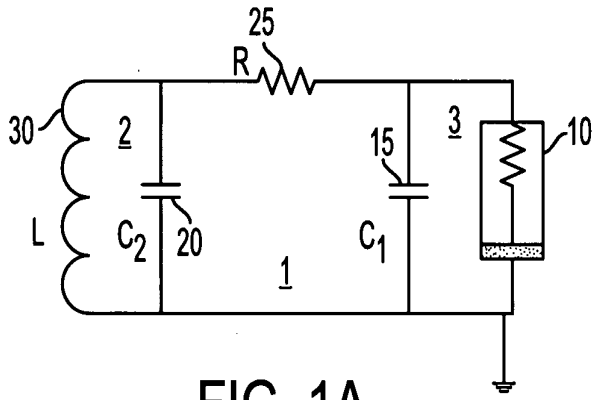


FIG. 1A
(PRIOR ART)

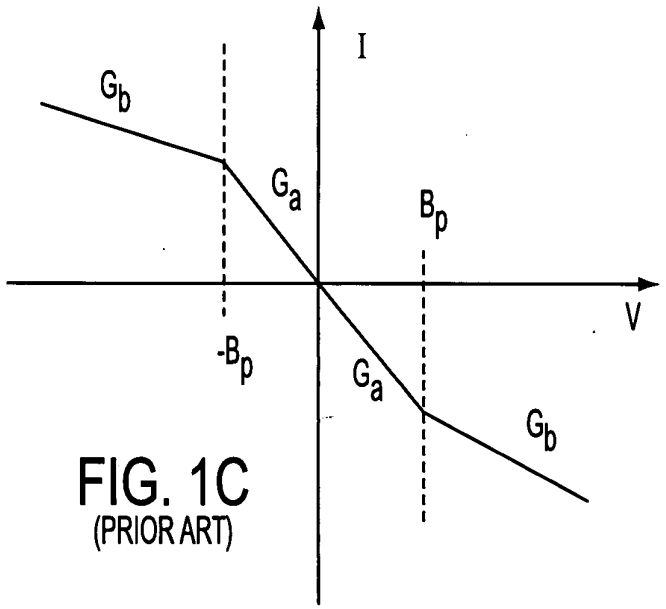


FIG. 1C
(PRIOR ART)

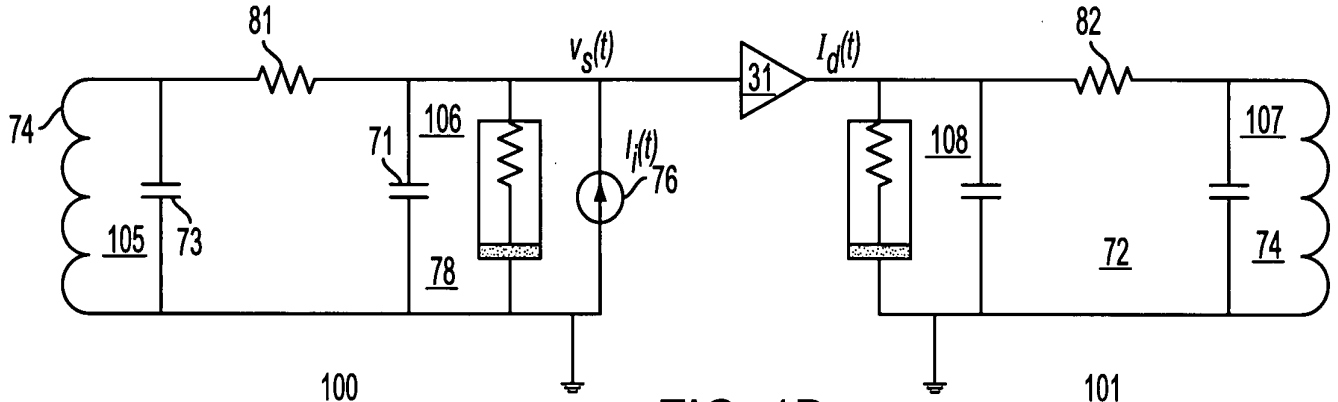


FIG. 1B
(PRIOR ART)

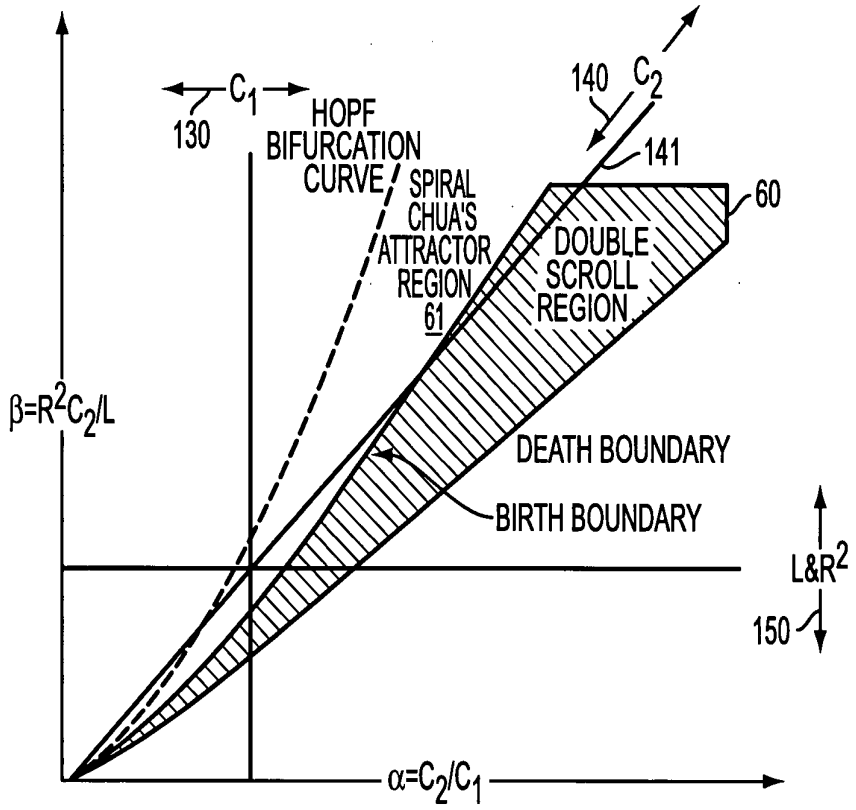

C_1
130
HOPF
BIFURCATION
CURVE
SPIRAL
CHUA'S
ATTRACTOR
REGION
61
140
C_2
141
60
DOUBLE
SCROLL
REGION
$\beta=R^2C_2/L$
DEATH BOUNDARY
BIRTH BOUNDARY
$L\&R^2$
150
$\alpha=C_2/C_1$

FIG. 1D

FIG. 2A

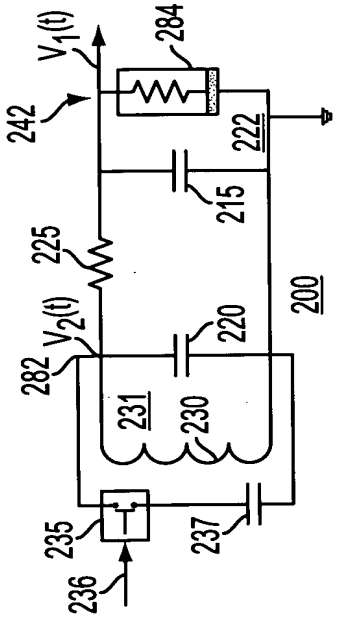
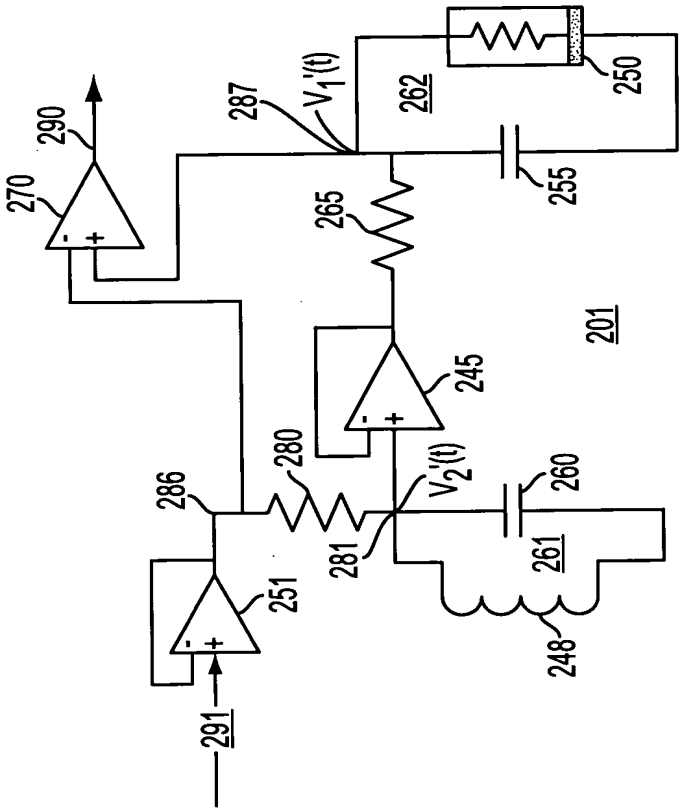


FIG. 2B
(PRIOR ART)



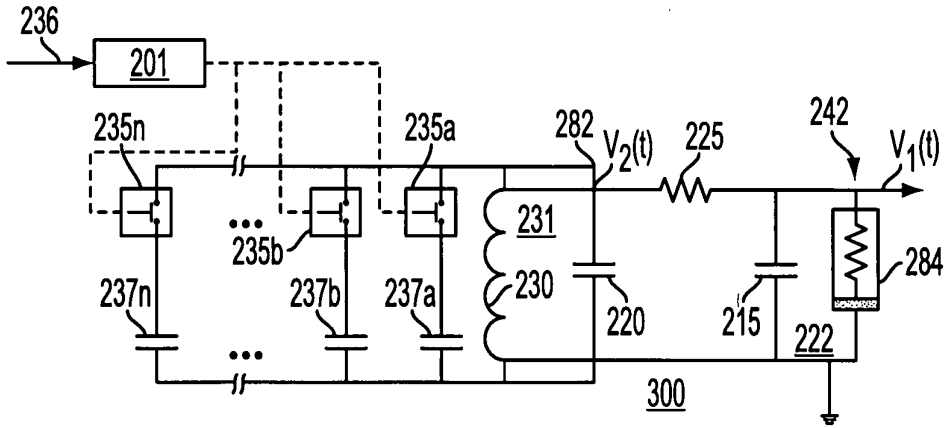

236
201
235n
235a
282
$V_2(t)$
225
242
$V_1(t)$
235b
231
230
284
237n
237b
237a
220
215
222
300

FIG. 3A

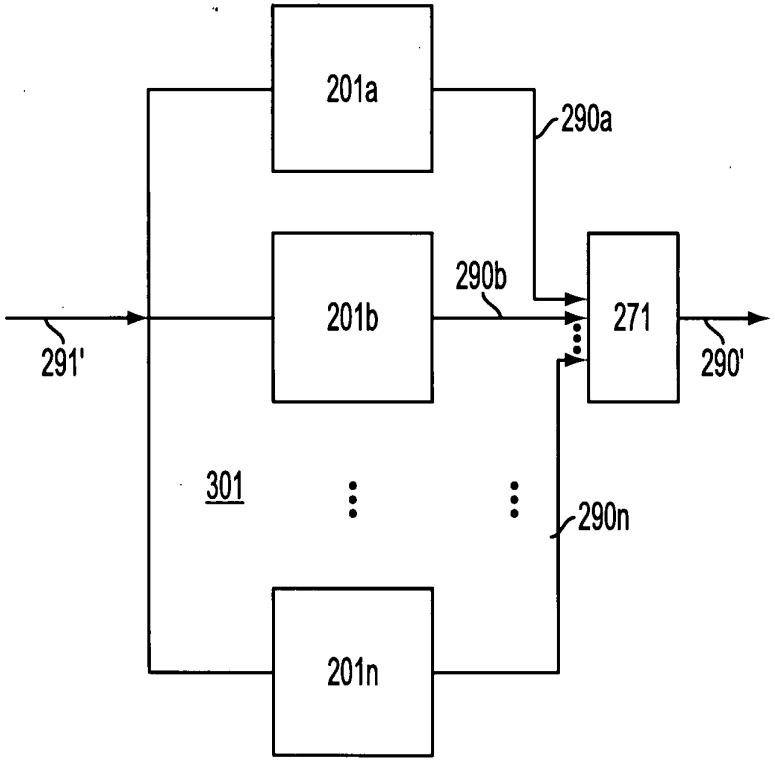

201a
290a
290b
201b
271
291'
290'
301
290n
201n

FIG. 3B

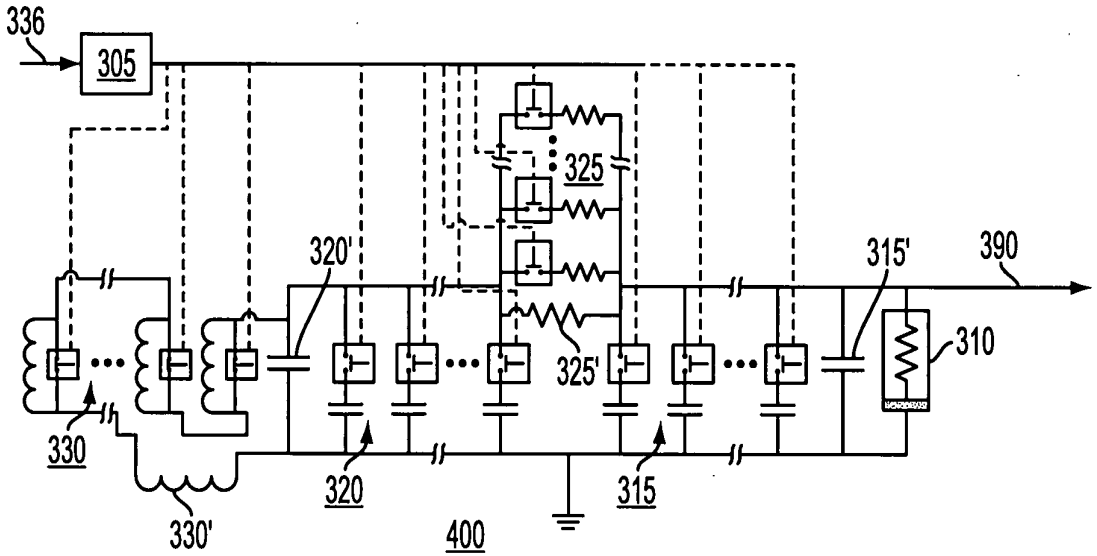

336
305
325
320'
315'
390
310
325'
330
320
315
330'
400

FIG. 4A

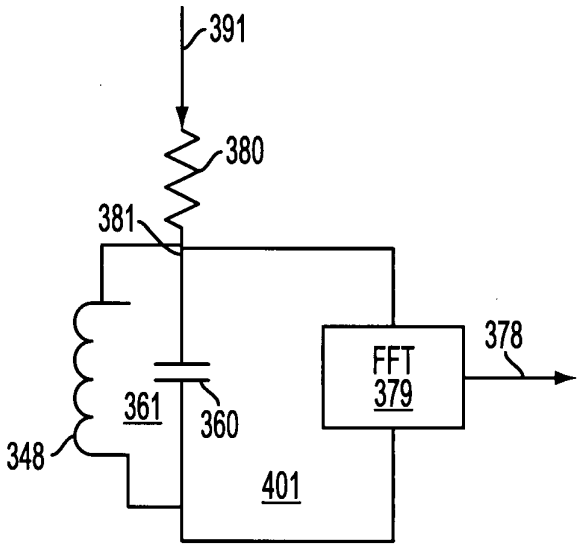

391
380
381
378
FFT
379
361
360
348
401

FIG. 4B

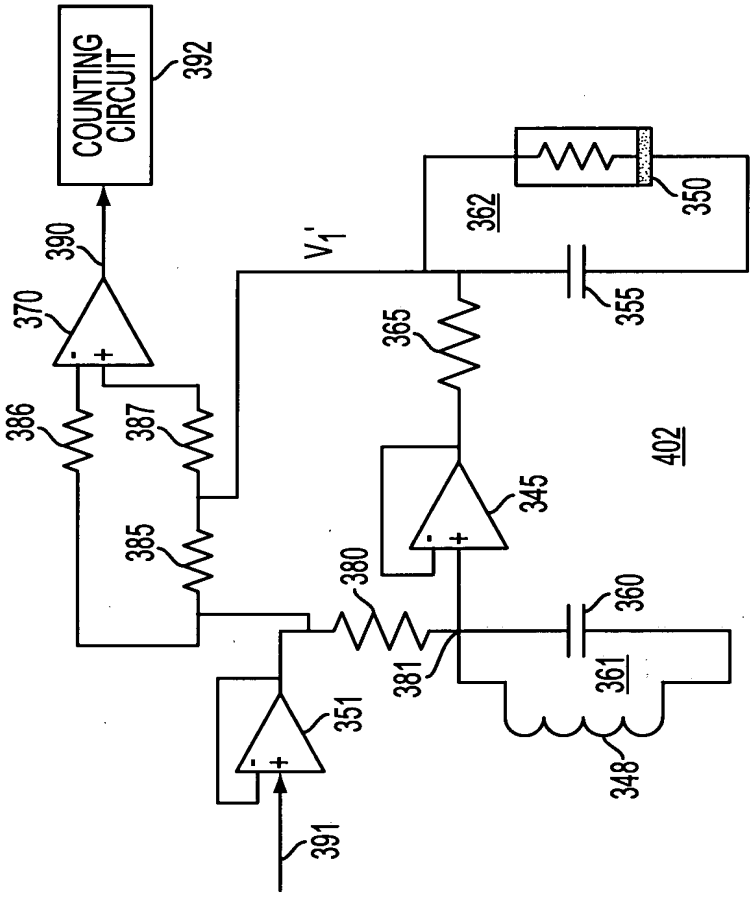

COUNTING CIRCUIT
392
390
370
386
387
385
380
381
351
391
345
365
362
350
355
360
361
348
402
V_1'

FIG. 4C

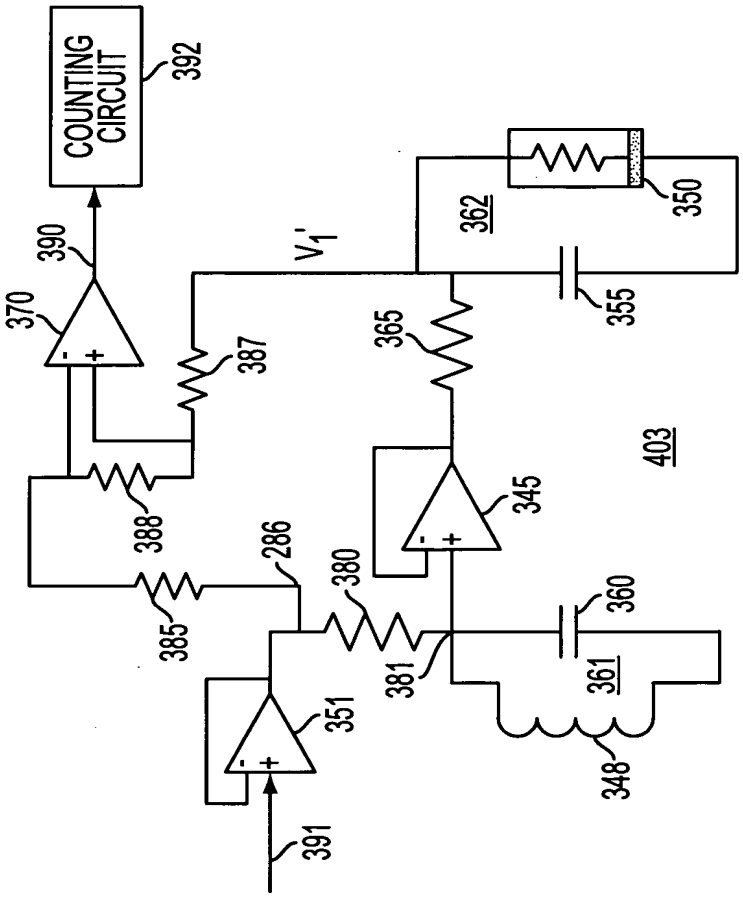

COUNTING CIRCUIT
392
390
370
387
V1'
362
350
355
365
345
403
388
286
380
360
385
381
361
351
348
391

FIG. 4D

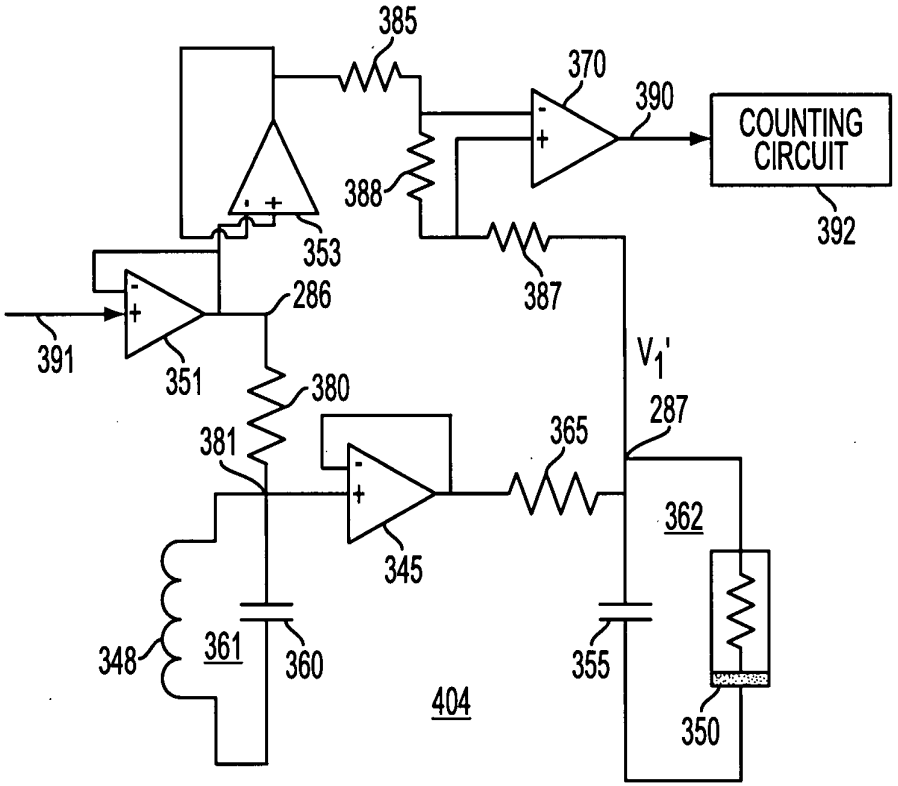

385
370
390
COUNTING CIRCUIT
388
392
353
387
286
391
351
V_1'
380
287
381
365
362
345
348
361
360
355
404
350

FIG. 4E

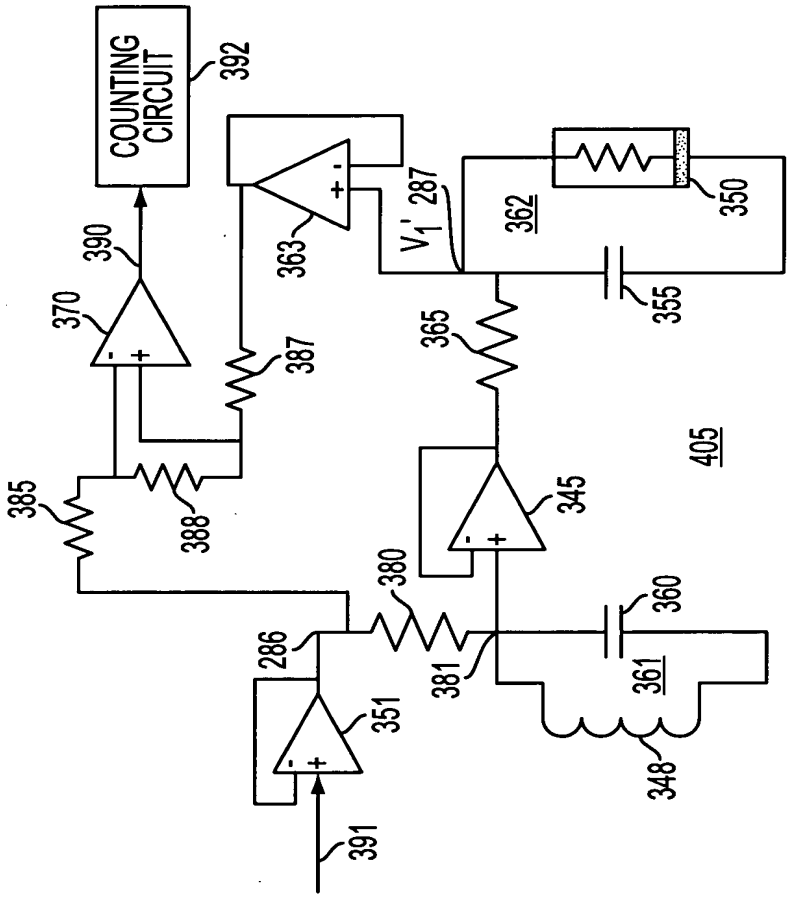

COUNTING CIRCUIT
392
390
370
387
385
388
363
287
V_1'
362
350
355
365
345
405
380
360
286
381
361
351
348
391

FIG. 4F

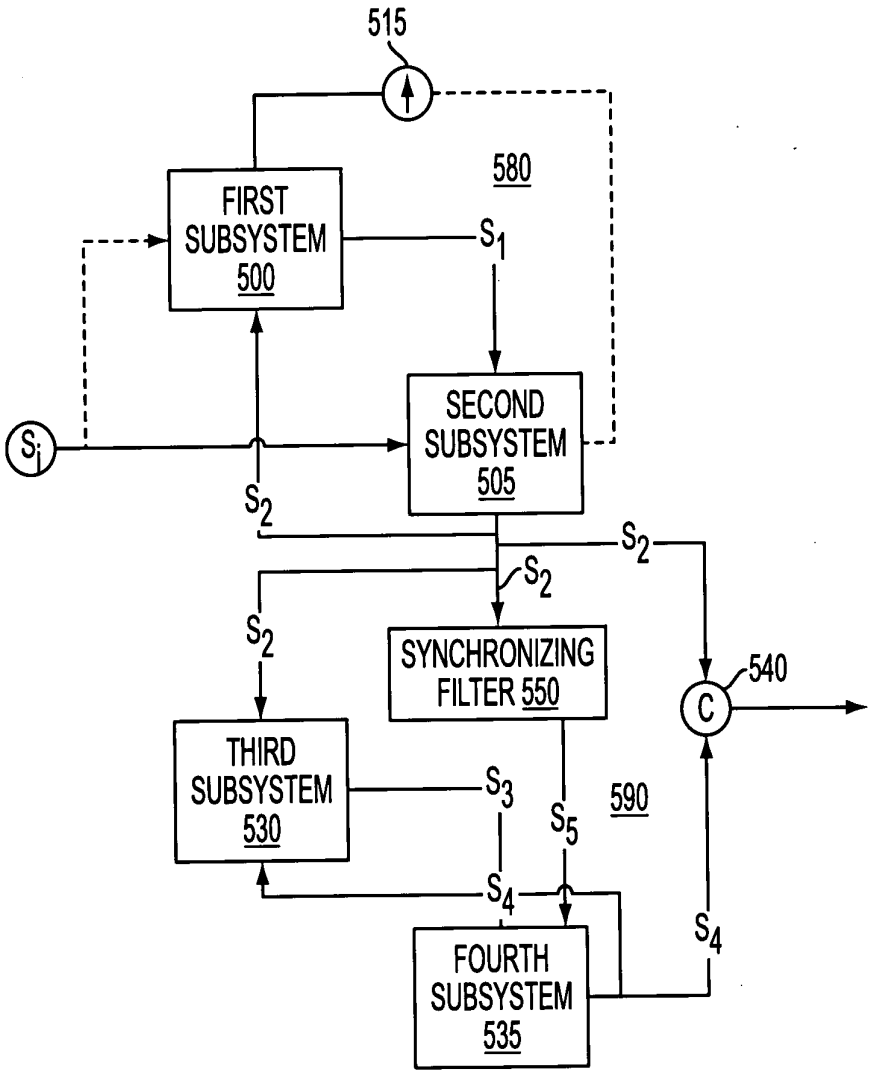

515
580
FIRST SUBSYSTEM 500
S_1
SECOND SUBSYSTEM 505
S_i
S_2
S_2
S_2
S_2
SYNCHRONIZING FILTER 550
540
C
THIRD SUBSYSTEM 530
S_3
590
S_5
S_4
S_4
FOURTH SUBSYSTEM 535

FIG. 5

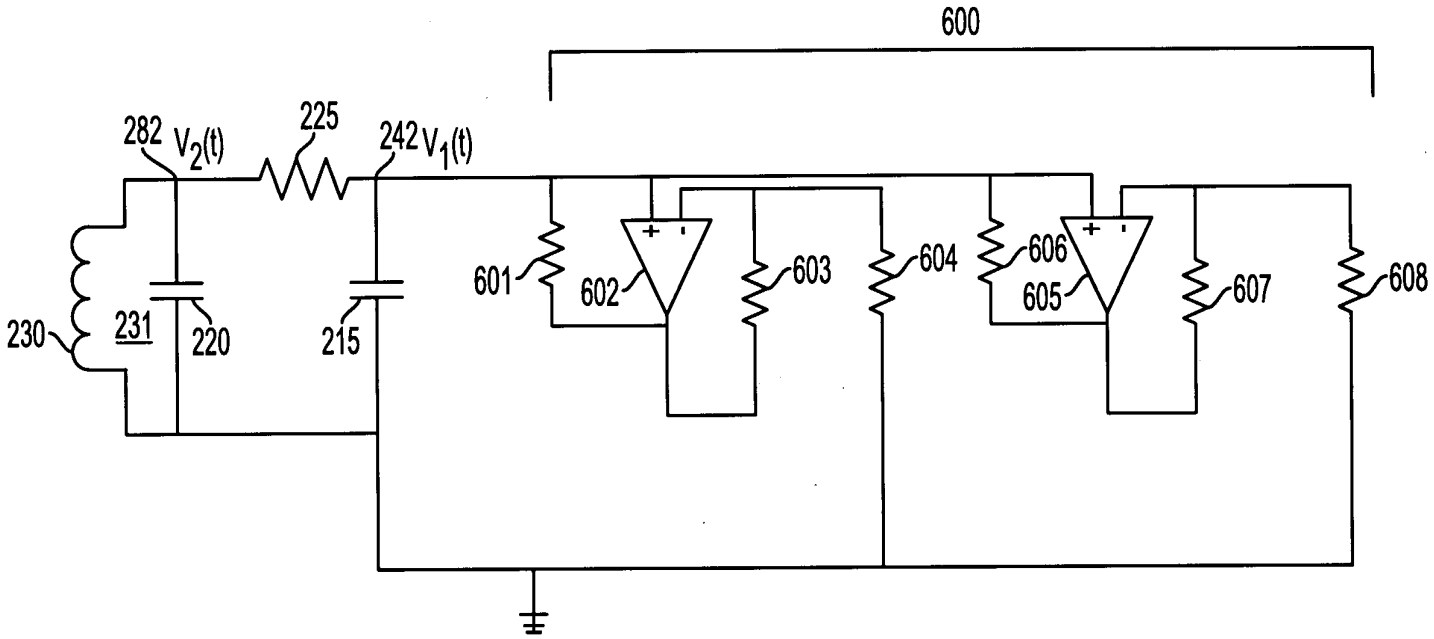


FIG. 6A
(PRIOR ART)

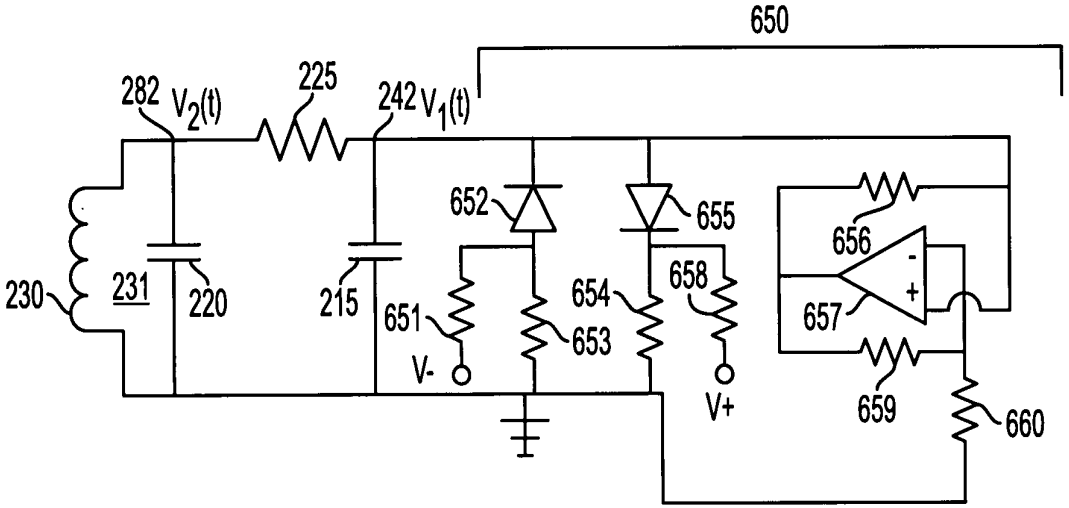


FIG. 6B
(PRIOR ART)

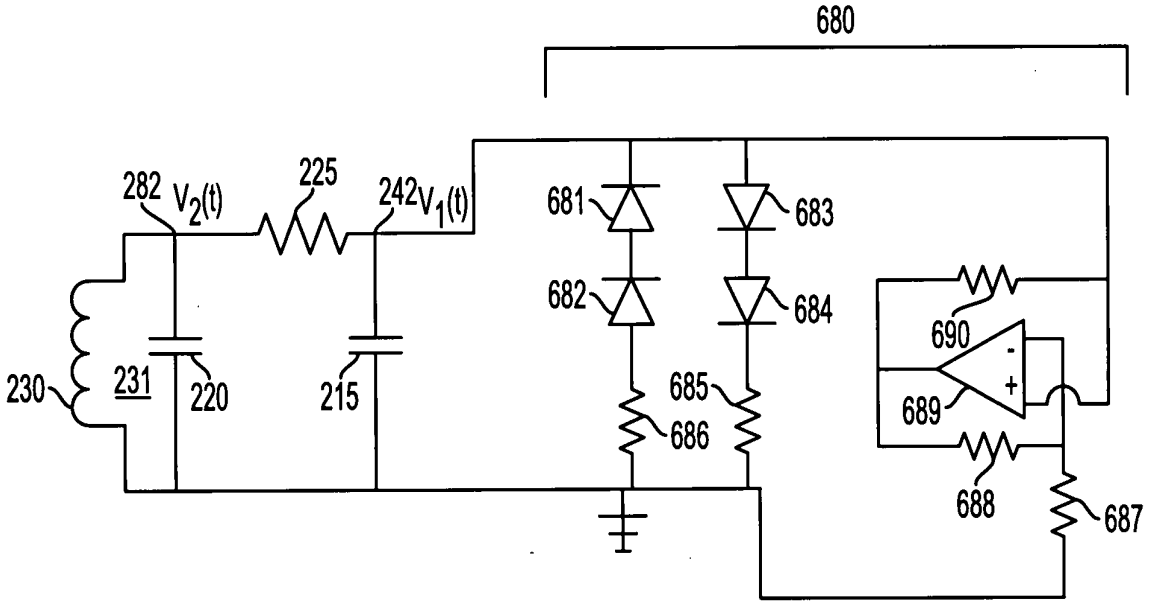

680
282
$V_2(t)$
225
242
$V_1(t)$
681
683
682
684
690
230
231
220
215
685
686
689
688
687

FIG. 6C

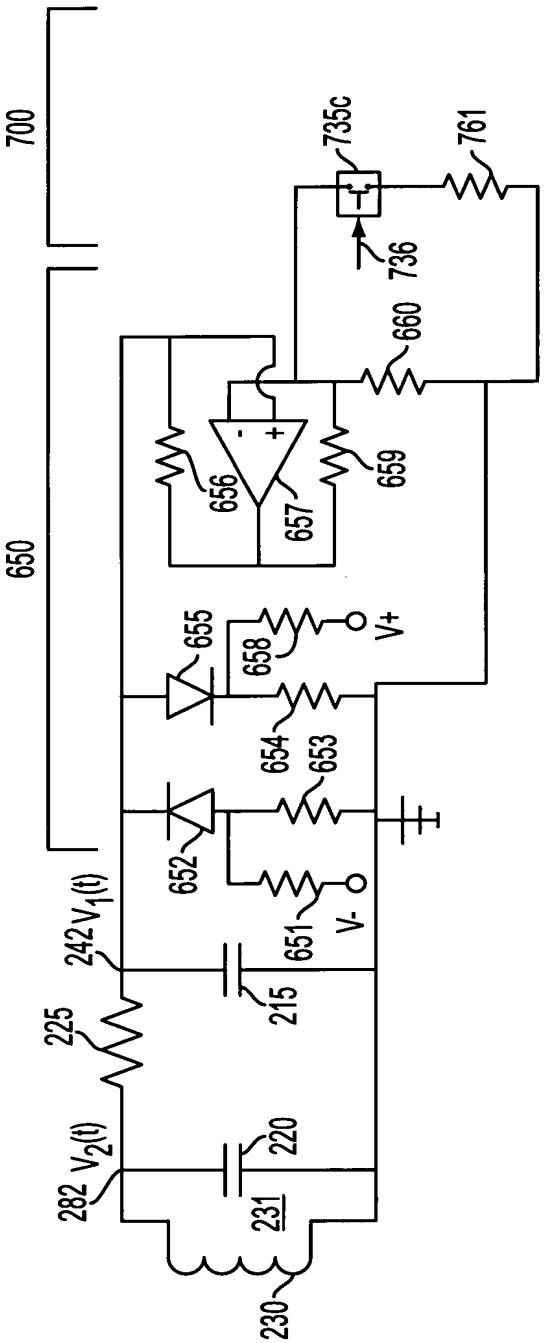

700
650
735c
761
736
660
656
657
659
655
658
V+
654
653
652
651
V-
242
$V_1(t)$
225
215
$V_2(t)$
282
220
231
230

FIG. 7A

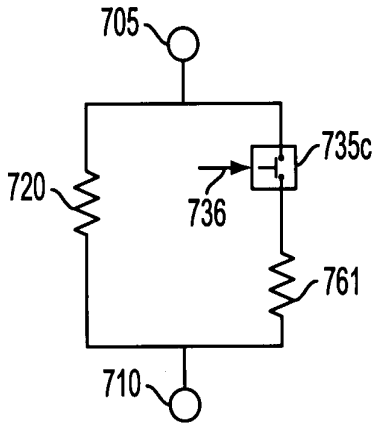


FIG. 7B

FIG. 6B CALTECH	R2'	R2	R1	R2'/R2	R2'/R2/R1
ELEMENT	653	654	660	653/654	653/654/660
G_a			X		X
G_b UPPER SCROLL		X	X	X	X
G_b LOWER SCROLL	X		X	X	X

$G_a = -1/R1$

$G_b = (R1-R2)/(R1*R2)$

FIG. 6A KENNEDY	R4	R5	R6	R1	R2	R3	R1/R3	R1/R2/R3	R5/R6	R1/R2/R3/R4
ELEMENT	601	603	604	606	607	608	606/608	606/608/607	603/604	606/607/608/601
G_a	X	X	X	X	X	X	X	X	X	X
G_b UPPER	X			X	X	X	X	X		X
G_b LOWER	X			X	X	X	X	X		X

$G_a = -(R2/(R1*R3)-(R5/(R4*R6)))$

$G_b = -(R2/(R1*R3)+(1/R4))$

FIG. 7C

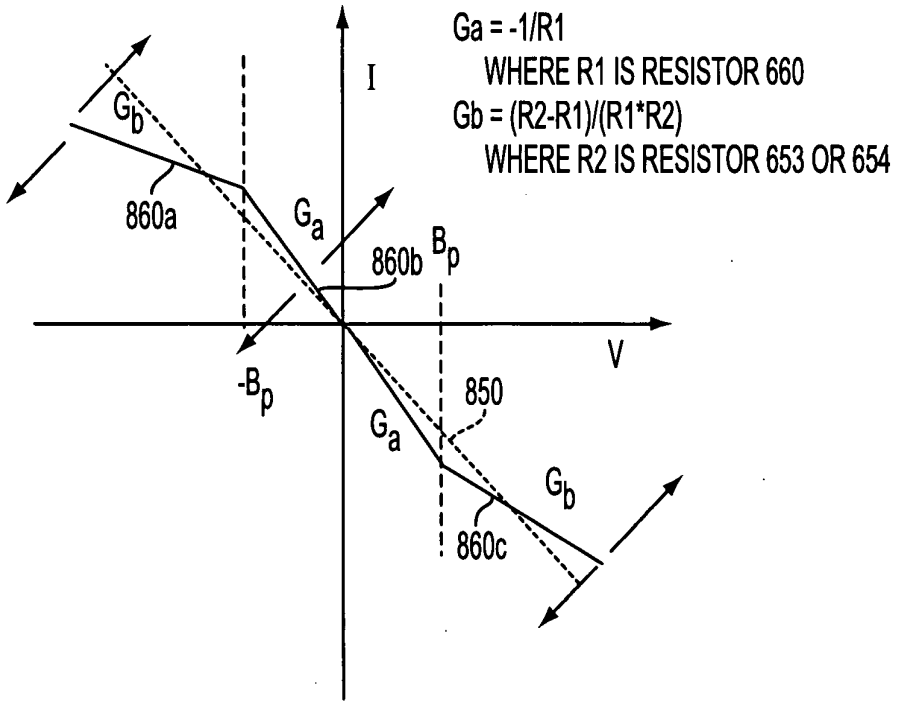

Ga = -1/R1
WHERE R1 IS RESISTOR 660
Gb = (R2-R1)/(R1*R2)
WHERE R2 IS RESISTOR 653 OR 654
I
V
Gb
860a
Ga
860b
Bp
-Bp
850
Ga
Gb
860c

FIG. 8

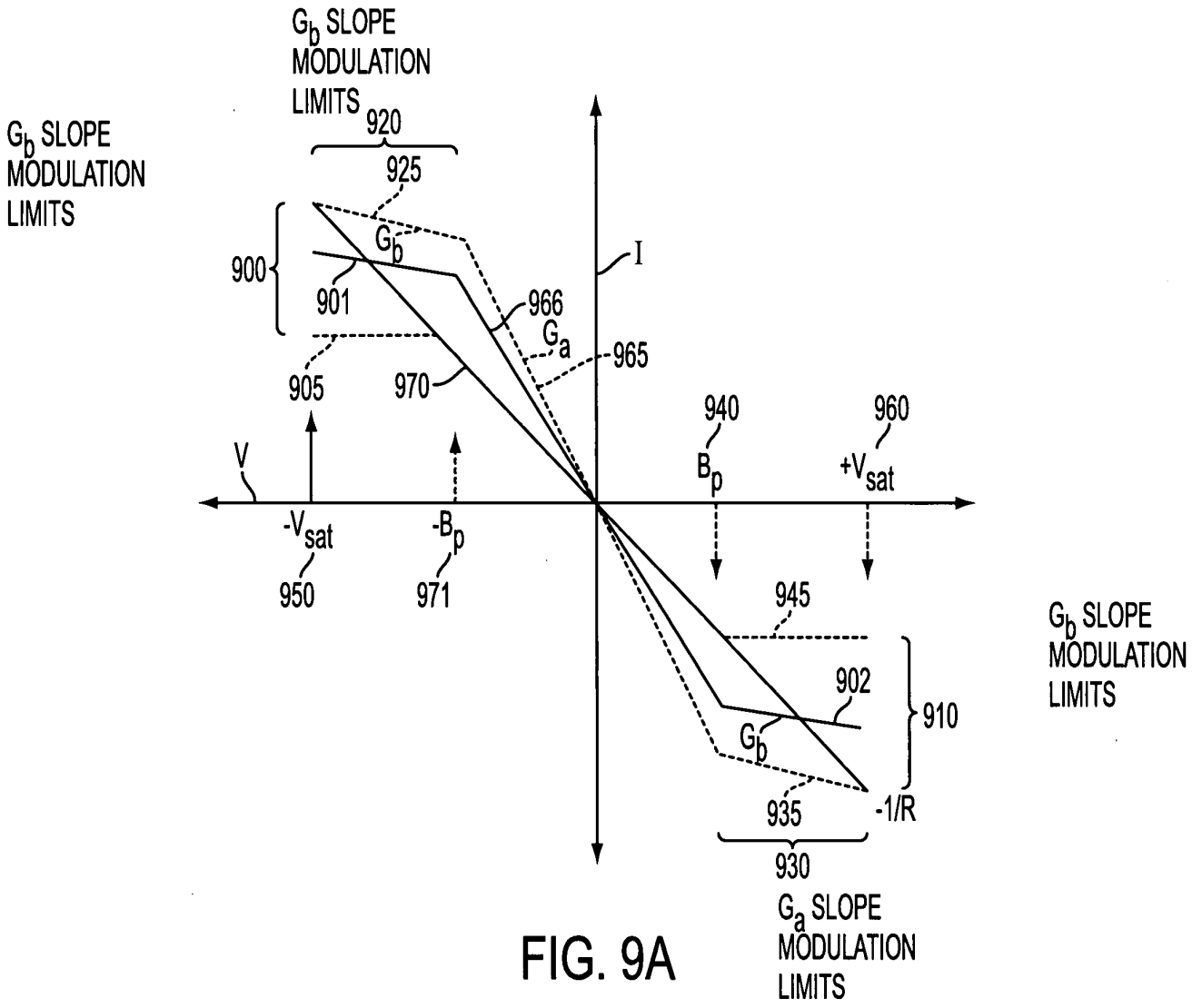

G_b SLOPE MODULATION LIMITS
G_b SLOPE MODULATION LIMITS
920
925
900
G_b
901
966
G_a
965
905
970
I
940
960
V
B_p
$+V_{sat}$
$-V_{sat}$
$-B_p$
950
971
945
902
910
G_b
935
-1/R
930
G_b SLOPE MODULATION LIMITS
G_a SLOPE MODULATION LIMITS

FIG. 9A

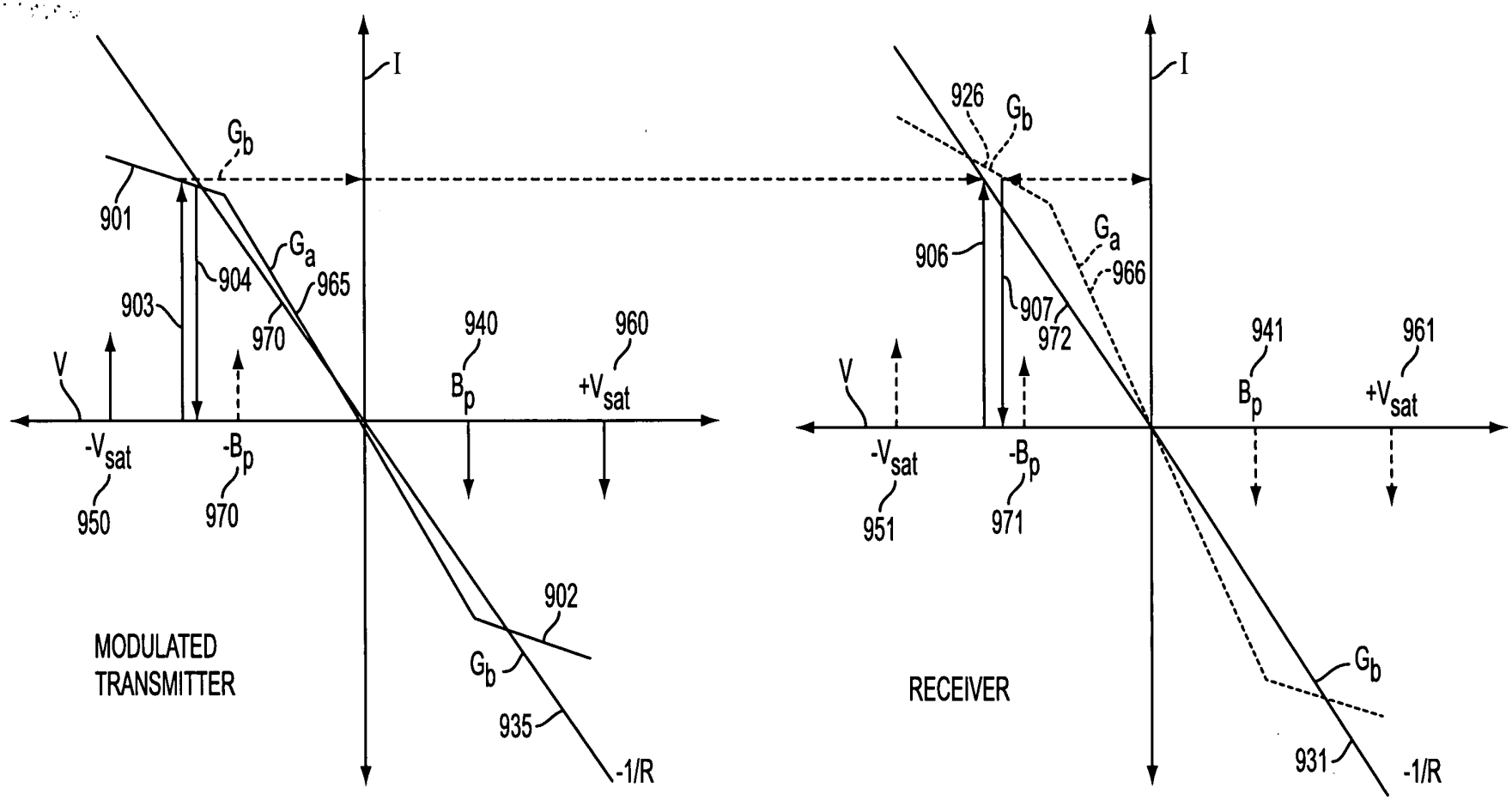

I
G_b
901
G_a
904
965
903
970
940
960
V
B_p
$+V_{sat}$
$-V_{sat}$
$-B_p$
950
970
902
G_b
935
-1/R
MODULATED
TRANSMITTER
926
G_b
906
G_a
966
907
972
941
961
V
B_p
$+V_{sat}$
$-V_{sat}$
$-B_p$
951
971
G_b
931
-1/R
RECEIVER

FIG. 9B

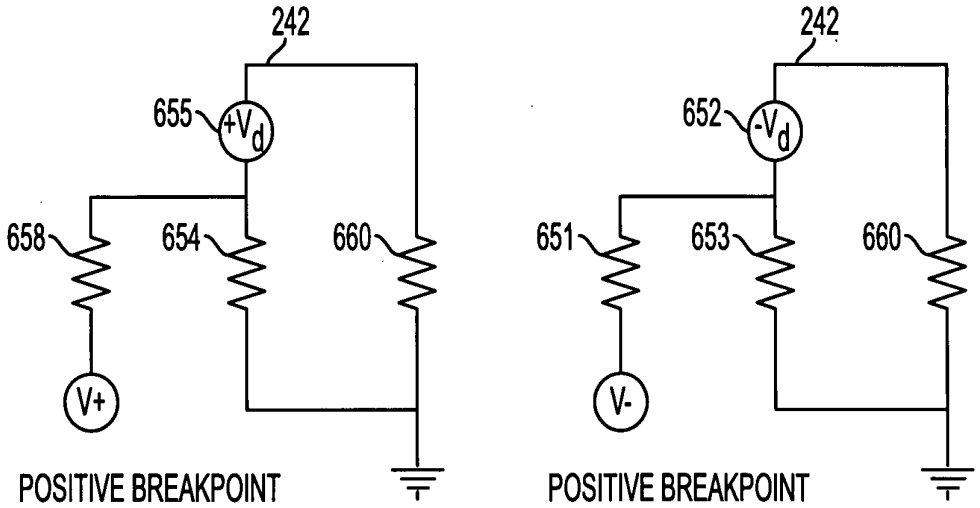

242
655
+Vd
658
654
660
V+
POSITIVE BREAKPOINT
242
652
-Vd
651
653
660
V-
POSITIVE BREAKPOINT

FIG. 9C

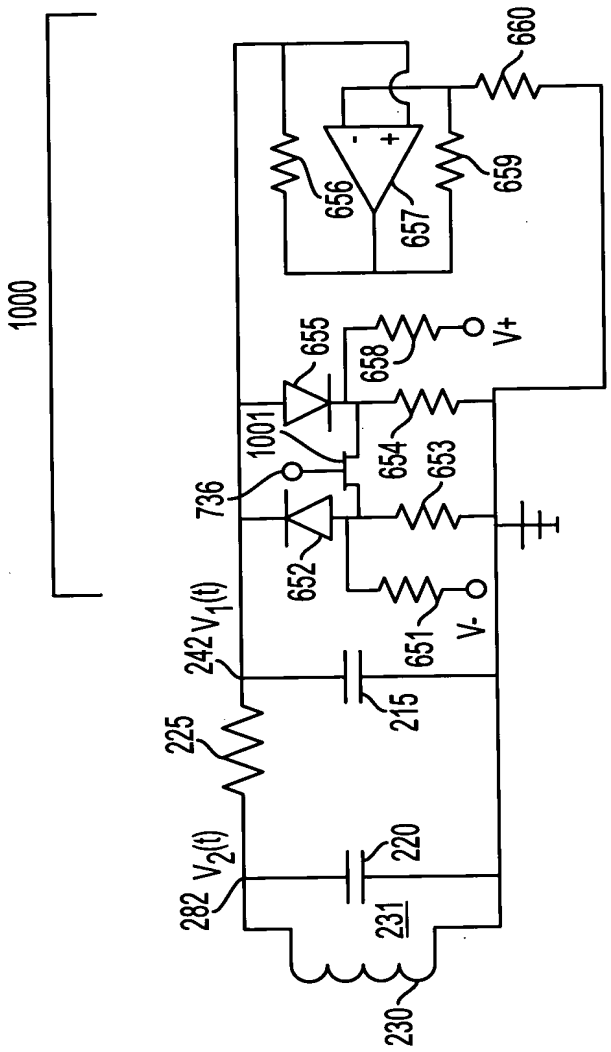

1000
660
656
657
659
655
658
V+
1001
654
653
736
652
651
V-
242
$V_1(t)$
215
225
220
282
$V_2(t)$
231
230

FIG. 10

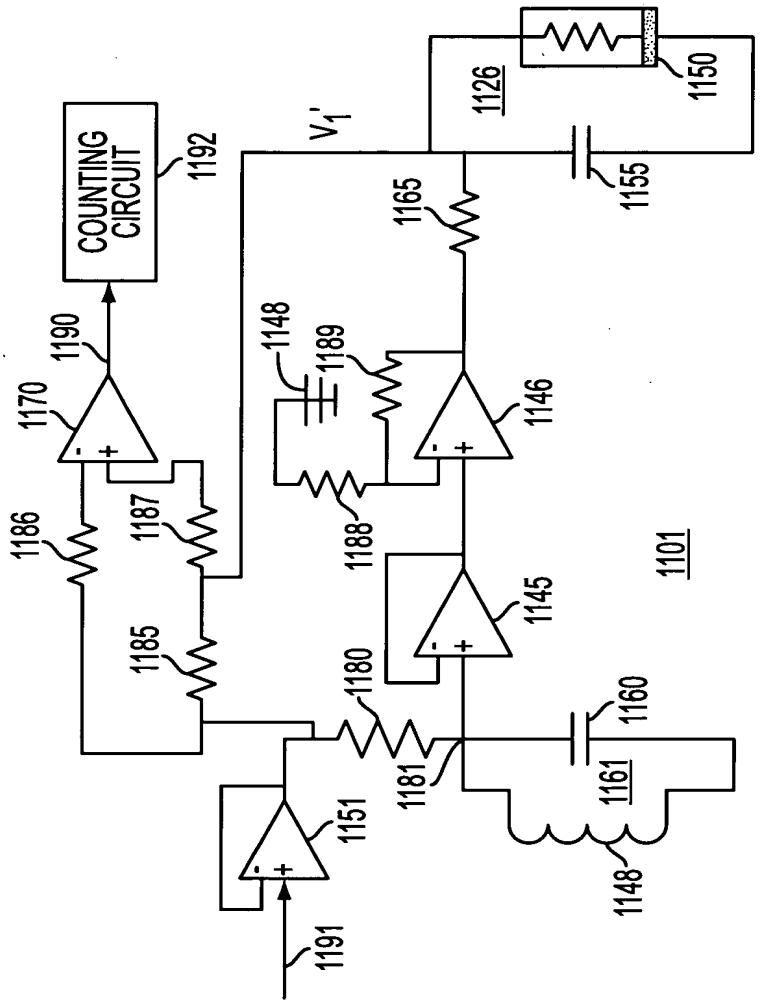

COUNTING CIRCUIT
1192
1190
1170
1186
1187
1185
1191
1151
1180
1181
1148
1189
1188
1146
1145
1160
1161
1148
1101
1126
1150
1155
1165
V_1'

FIG. 11

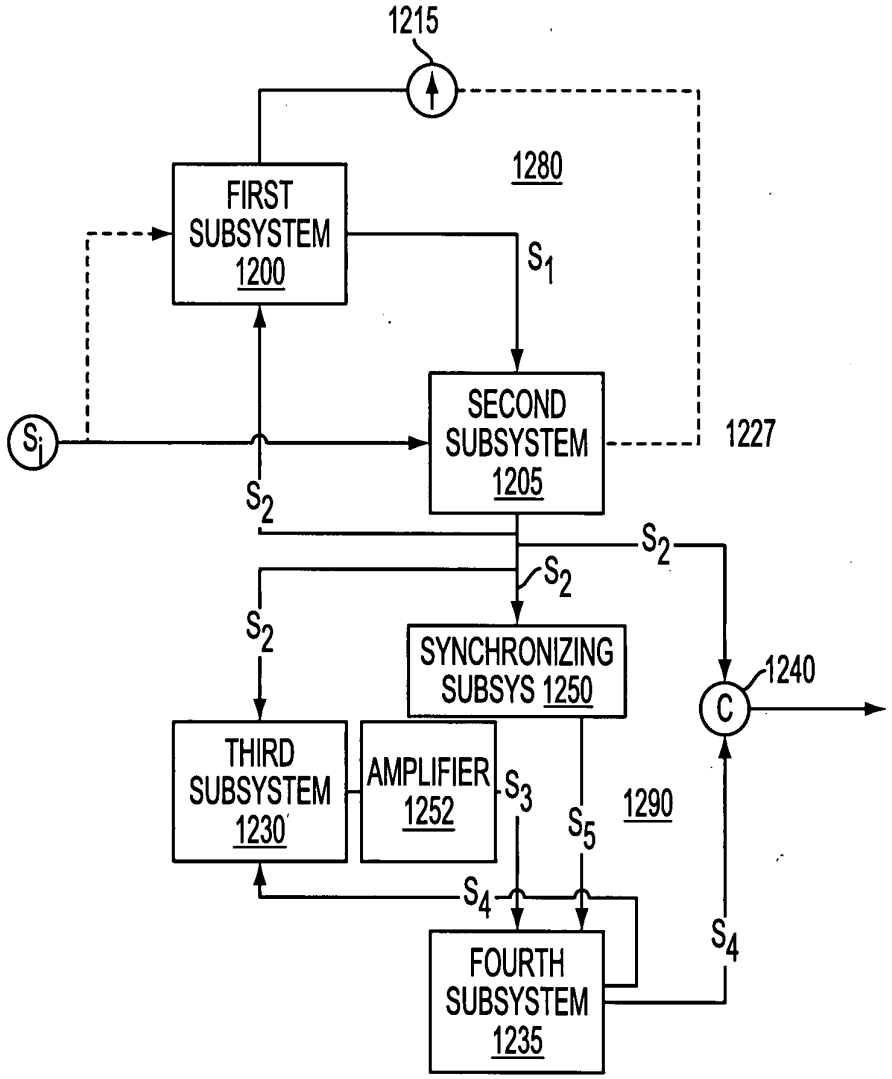

1215
1280
FIRST SUBSYSTEM 1200
S_1
SECOND SUBSYSTEM 1205
1227
S_i
S_2
S_2
S_2
S_2
SYNCHRONIZING SUBSYS 1250
1240
C
THIRD SUBSYSTEM 1230'
AMPLIFIER 1252
S_3
S_5
1290
S_4
S_4
FOURTH SUBSYSTEM 1235

FIG. 12

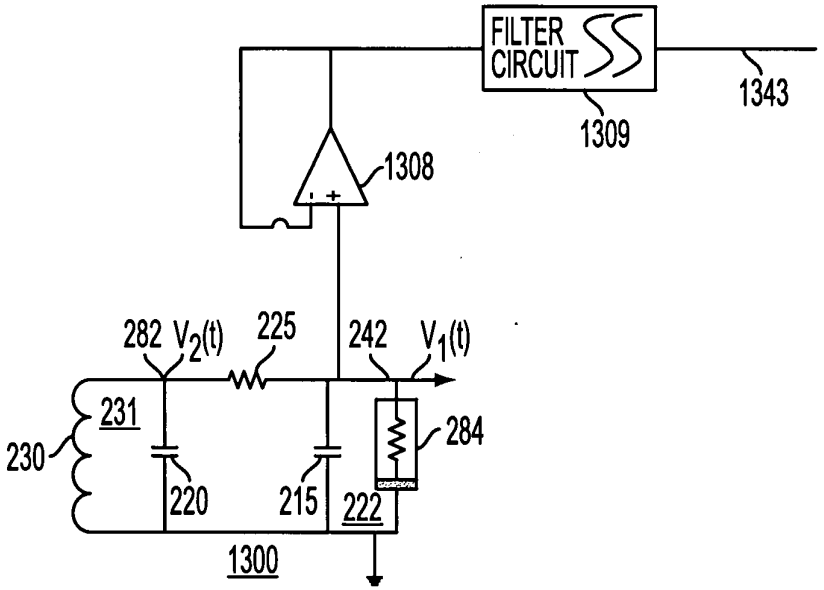

FILTER CIRCUIT
1343
1309
1308
282
$V_2(t)$
225
242
$V_1(t)$
231
230
284
220
215
222
1300

FIG. 13

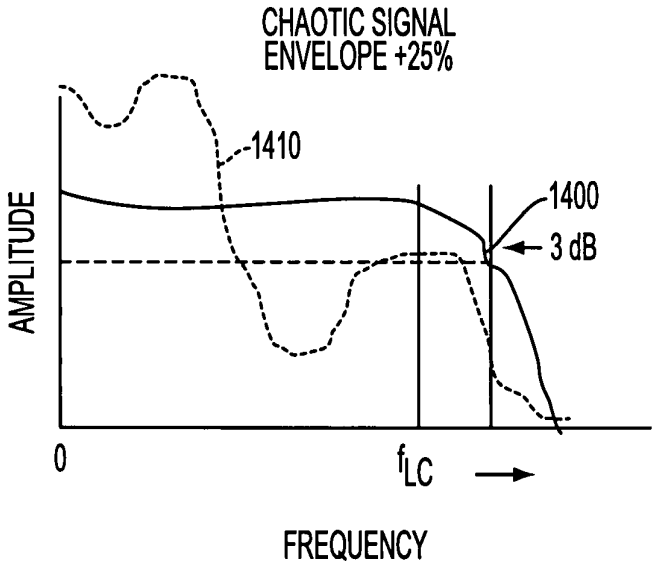


FIG. 14A

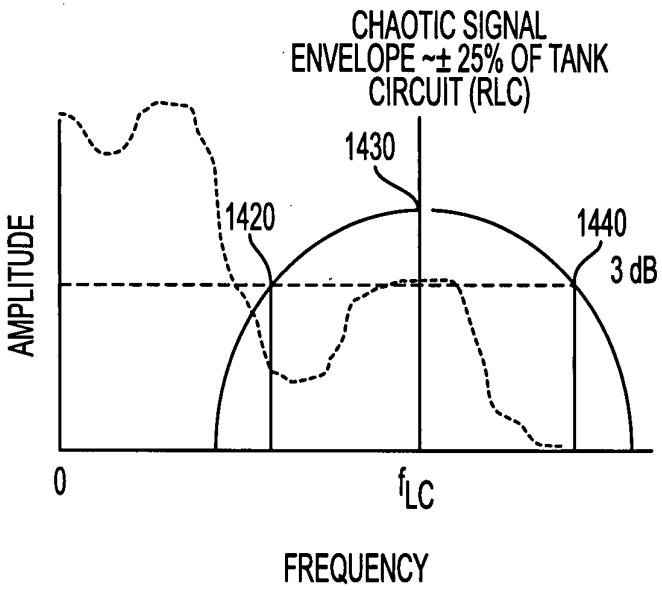


FIG. 14B

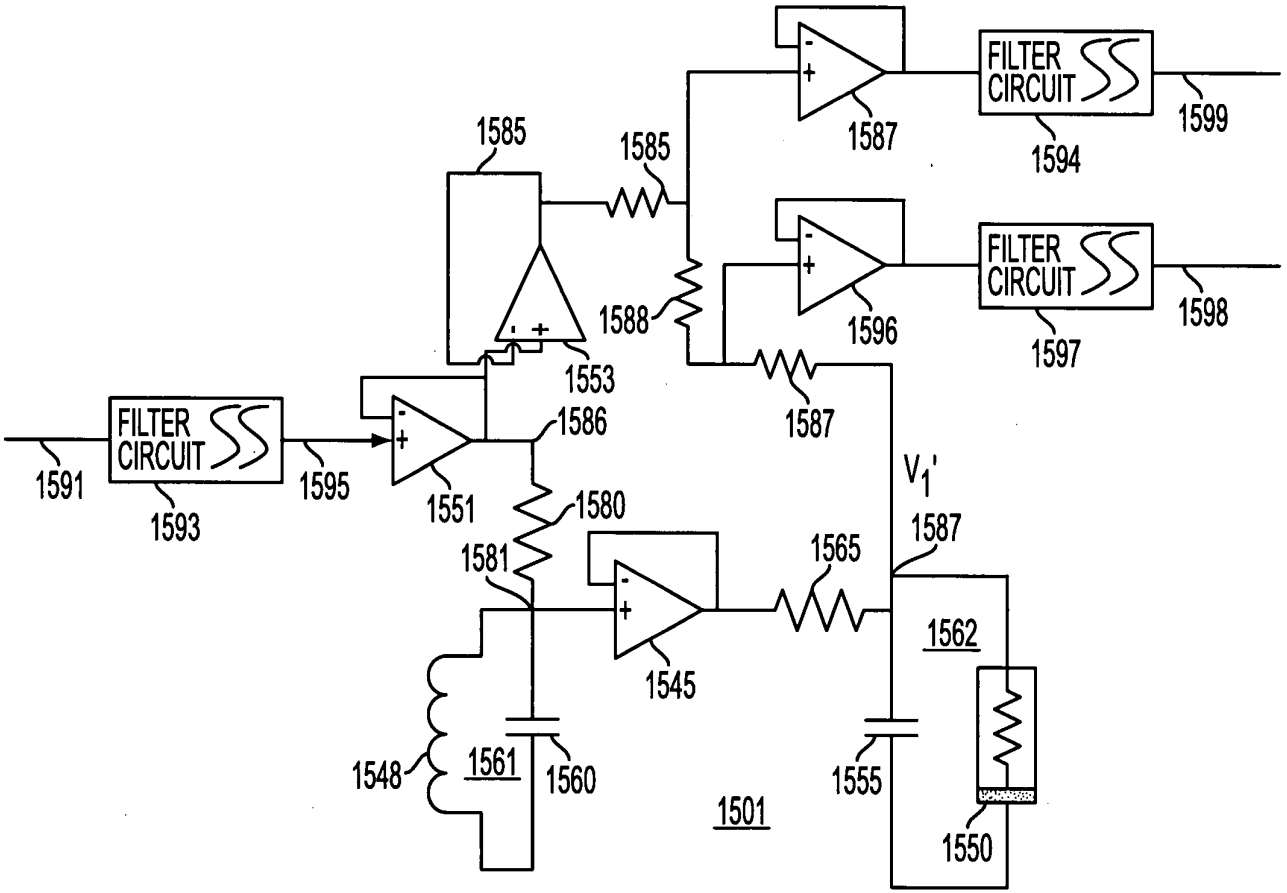

FILTER CIRCUIT
1591
1593
1595
1551
1586
1585
1585
1553
1588
1587
1587
1594
1599
1596
1598
1597
1580
1581
1565
1587
V_1'
1562
1545
1548
1561
1560
1555
1550
1501

FIG. 15

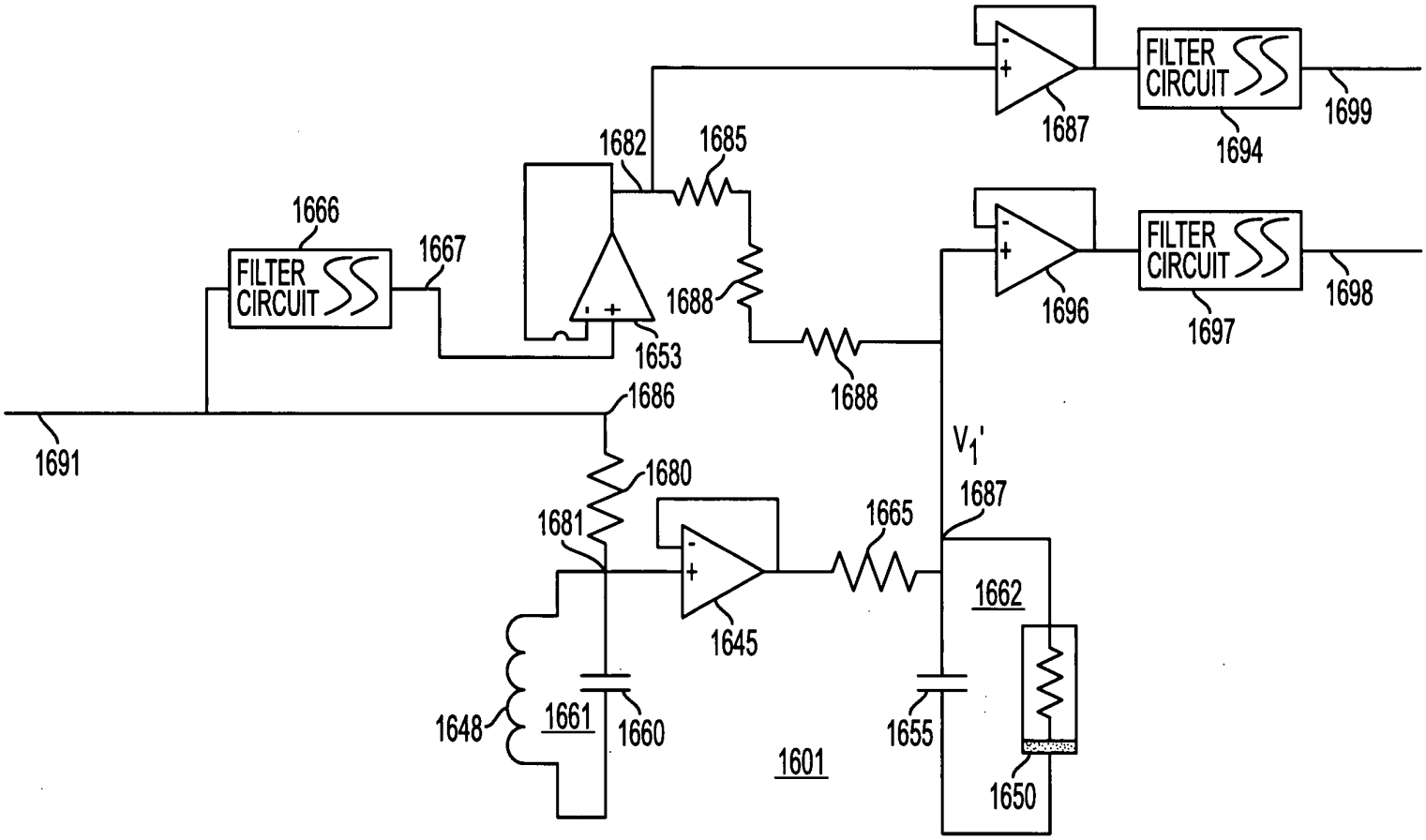

FILTER CIRCUIT
1666
1667
1682
1685
1687
1694
1699
1696
1697
1698
1688
1653
1686
1691
1680
1681
1665
1645
1662
1661
1660
1648
1655
1650
1601
V_1'

FIG. 16

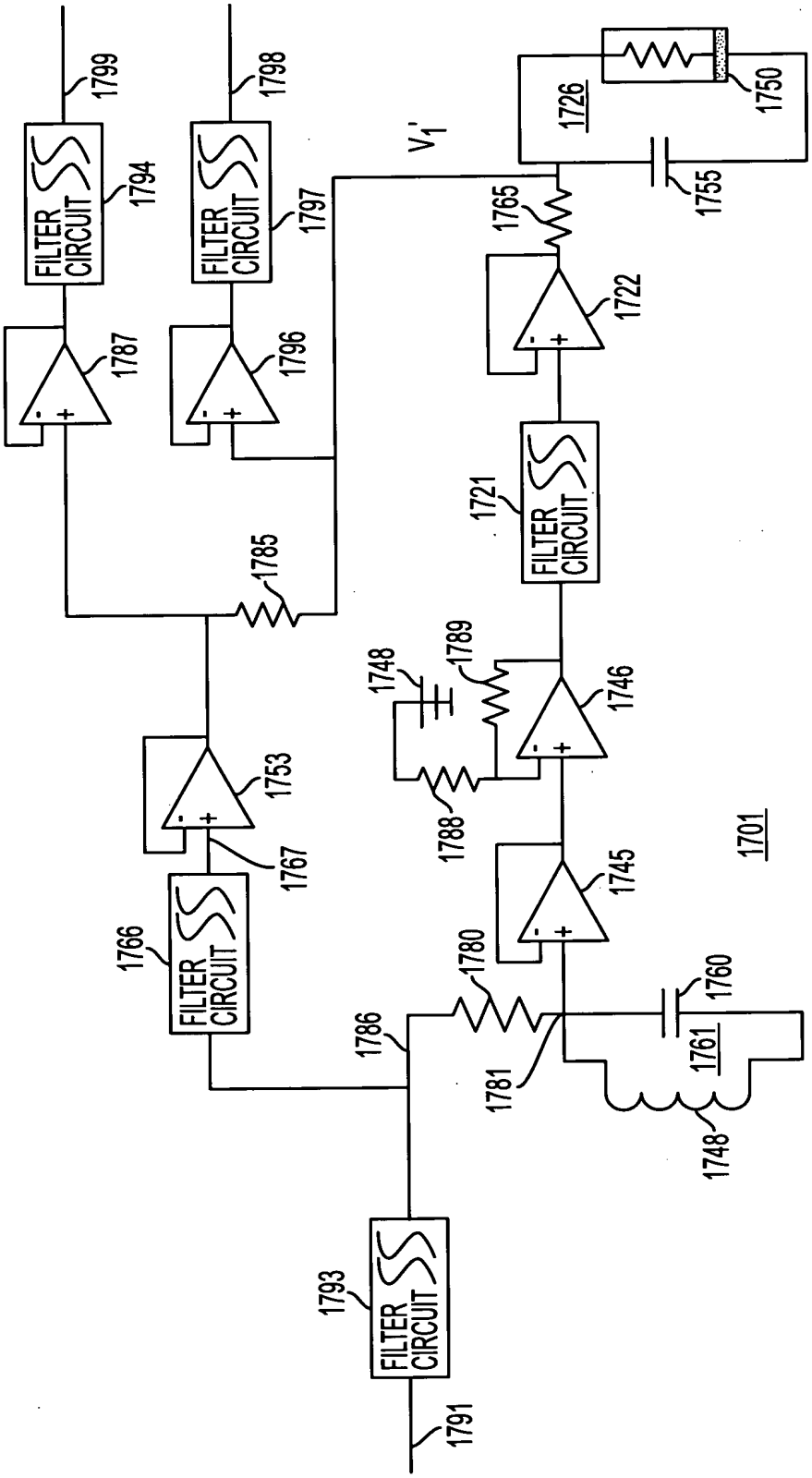

1799
1798
FILTER CIRCUIT
1794
1797
1787
1796
V1'
1726
1750
1755
1765
1722
1721
1785
1789
1748
1746
1753
1788
1767
1745
1701
1766
1780
1760
1786
1761
1781
1748
1793
1791

FIG. 17

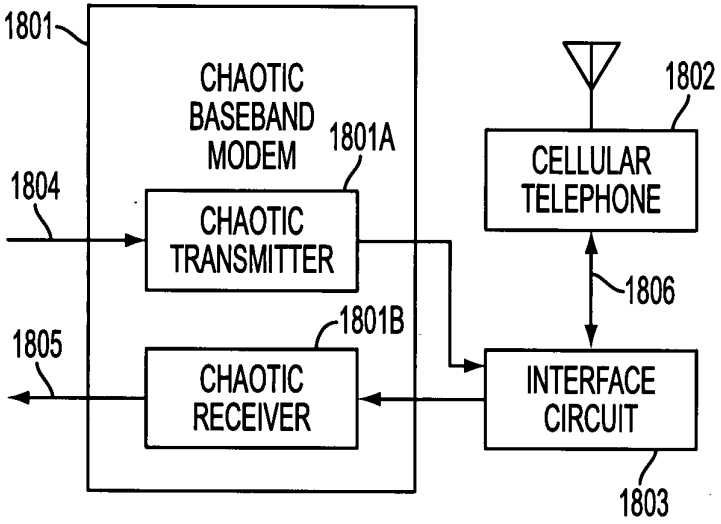


FIG. 18A

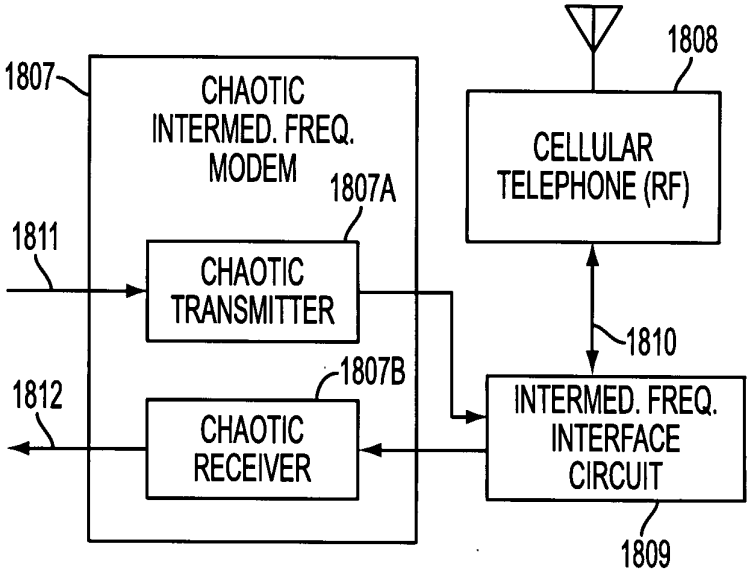


FIG. 18B

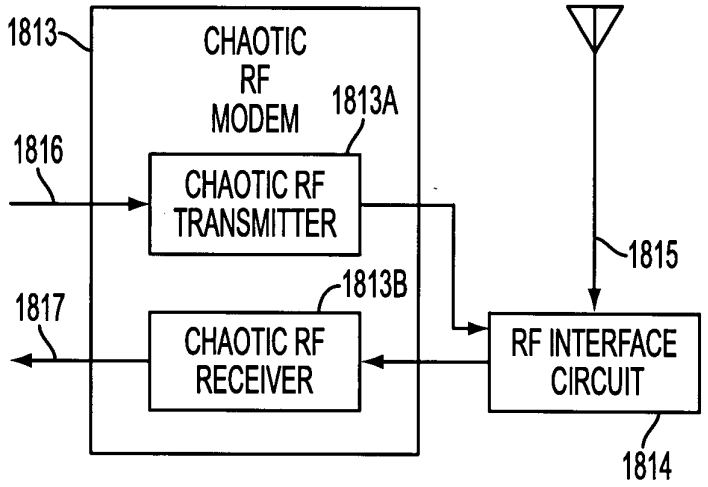


FIG. 18C

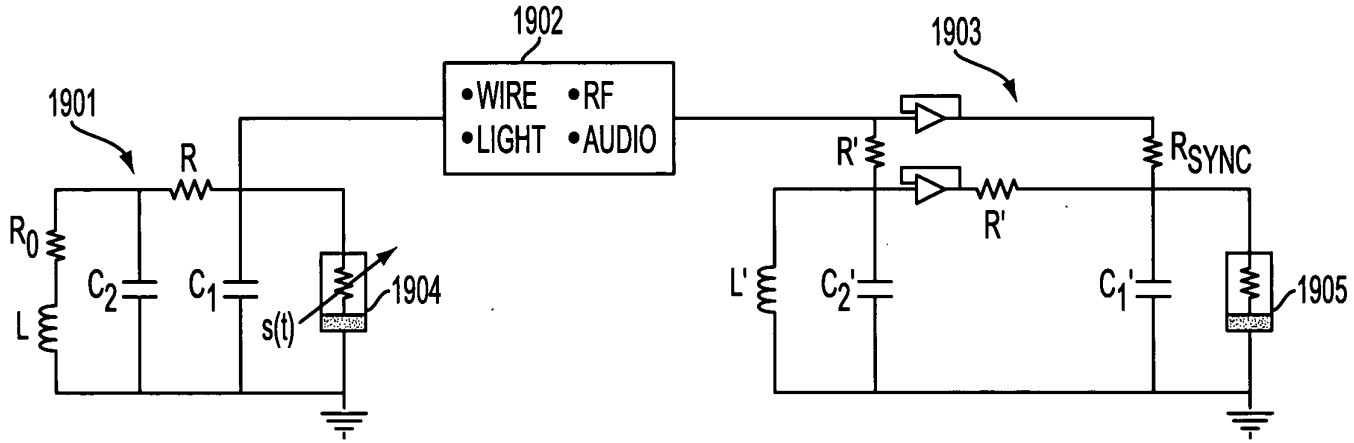


FIG. 19A

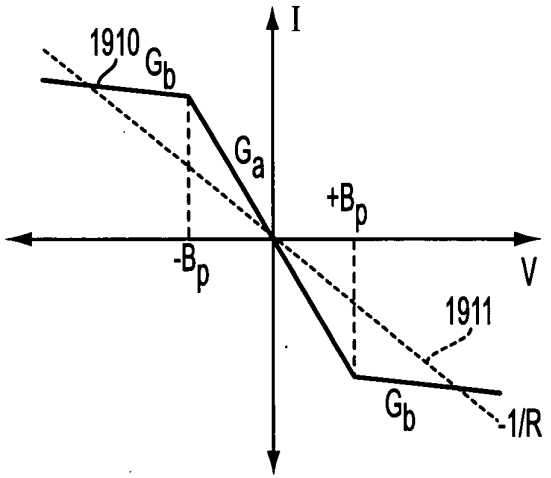


FIG. 19B

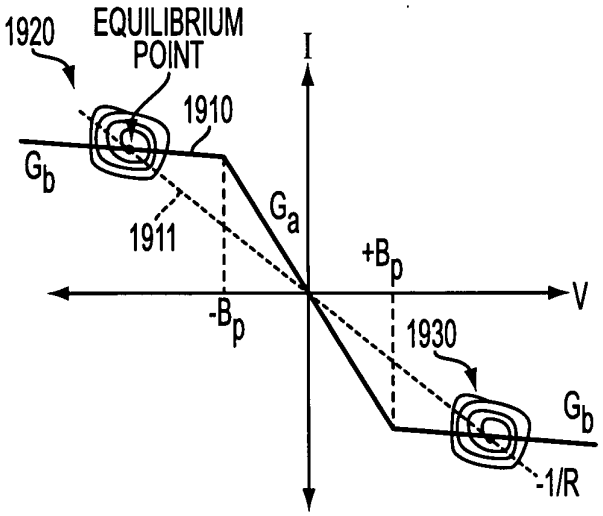


FIG. 19C

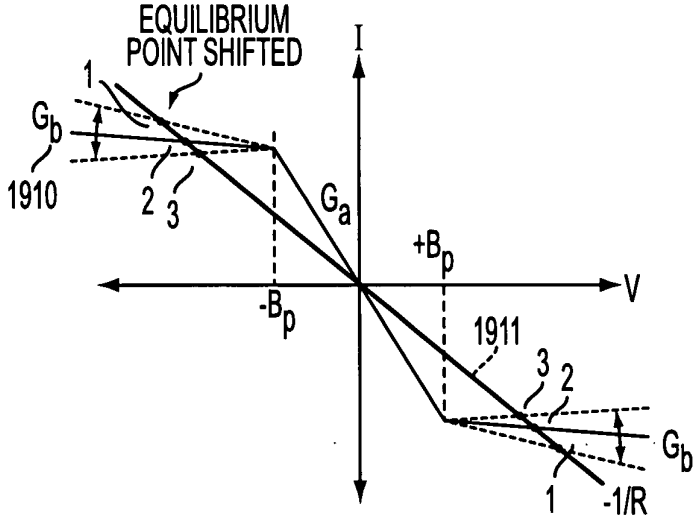


FIG. 19D

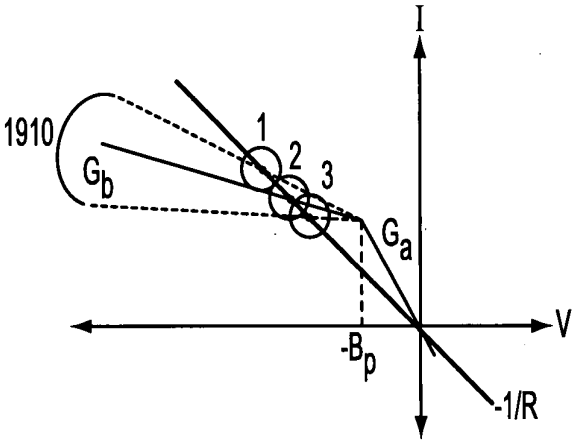


FIG. 19E

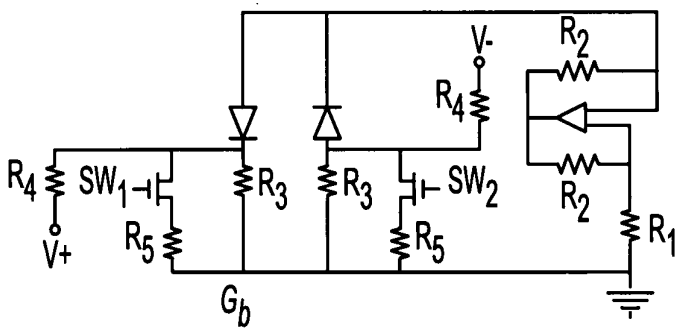


FIG. 19F

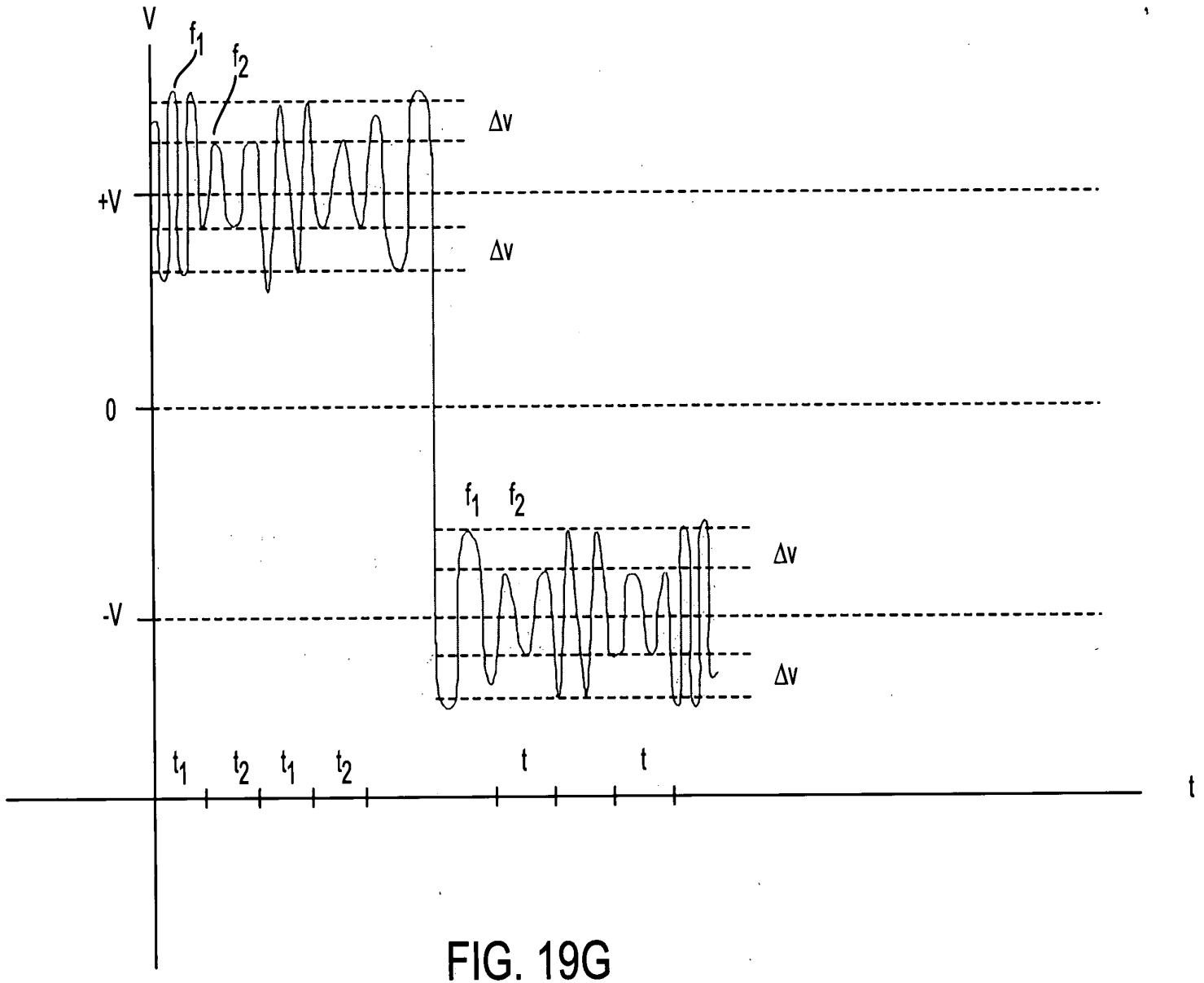


FIG. 19G

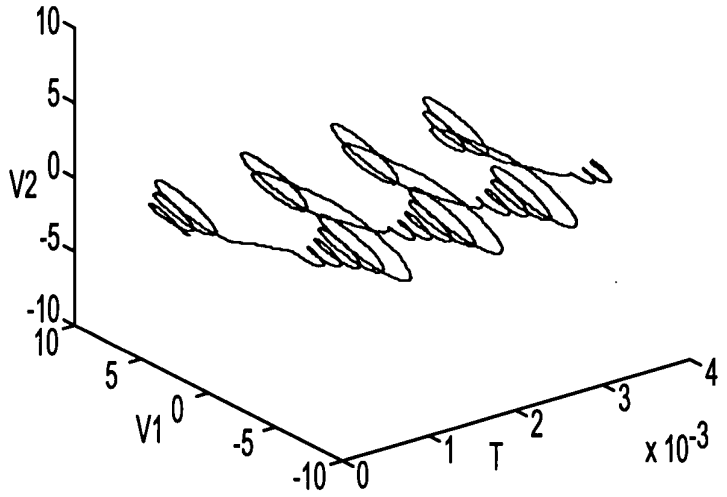


FIG. 20A

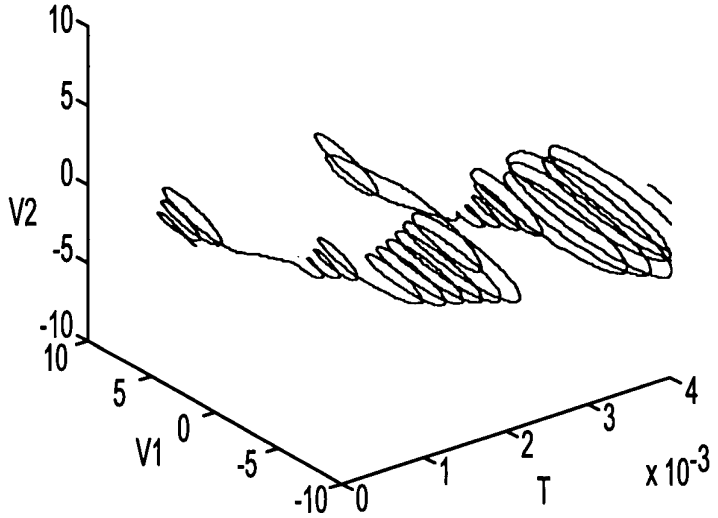


FIG. 20B

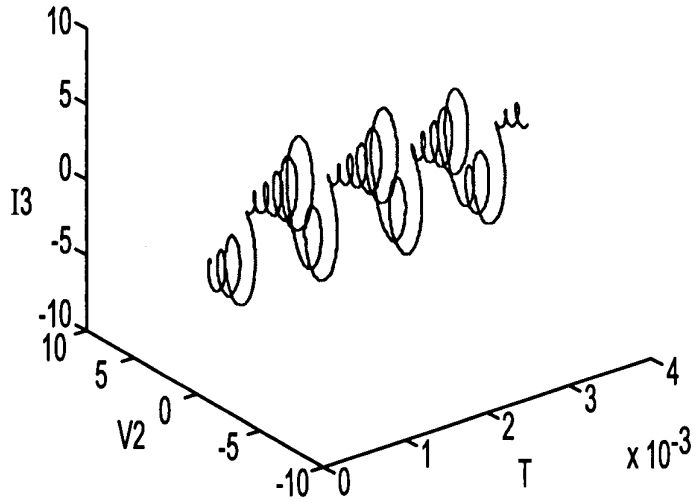


FIG. 20C

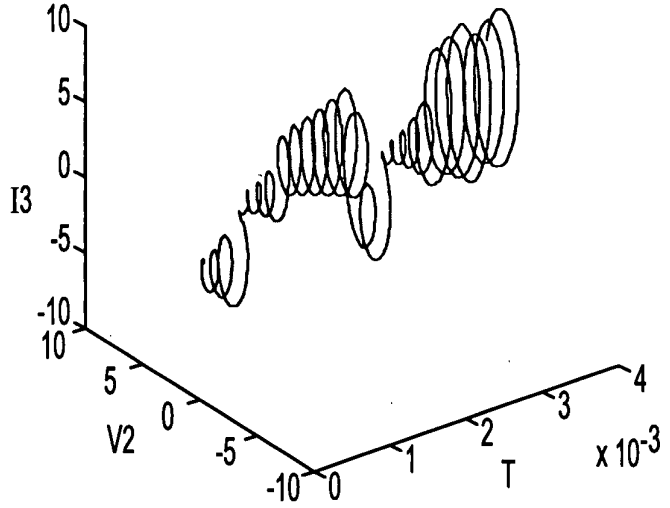


FIG. 20D

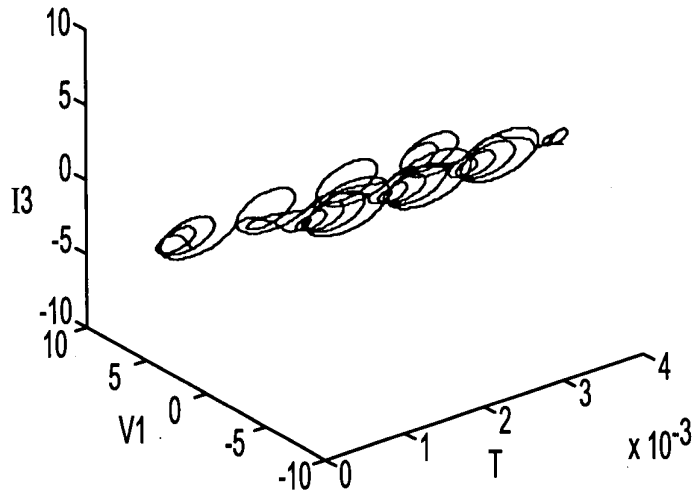


FIG. 20E

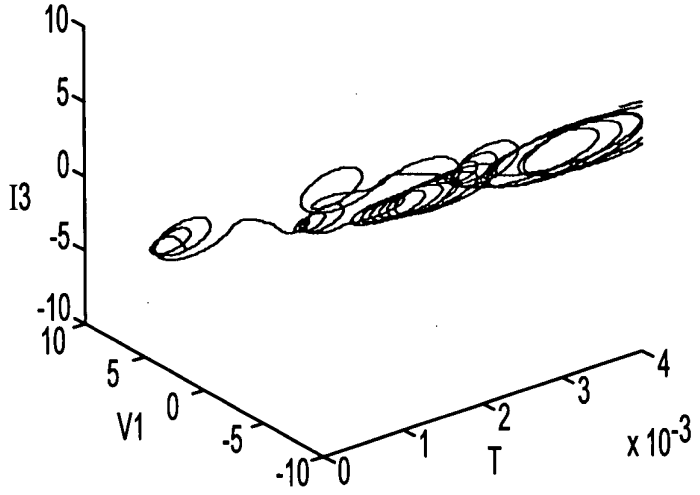


FIG. 20F

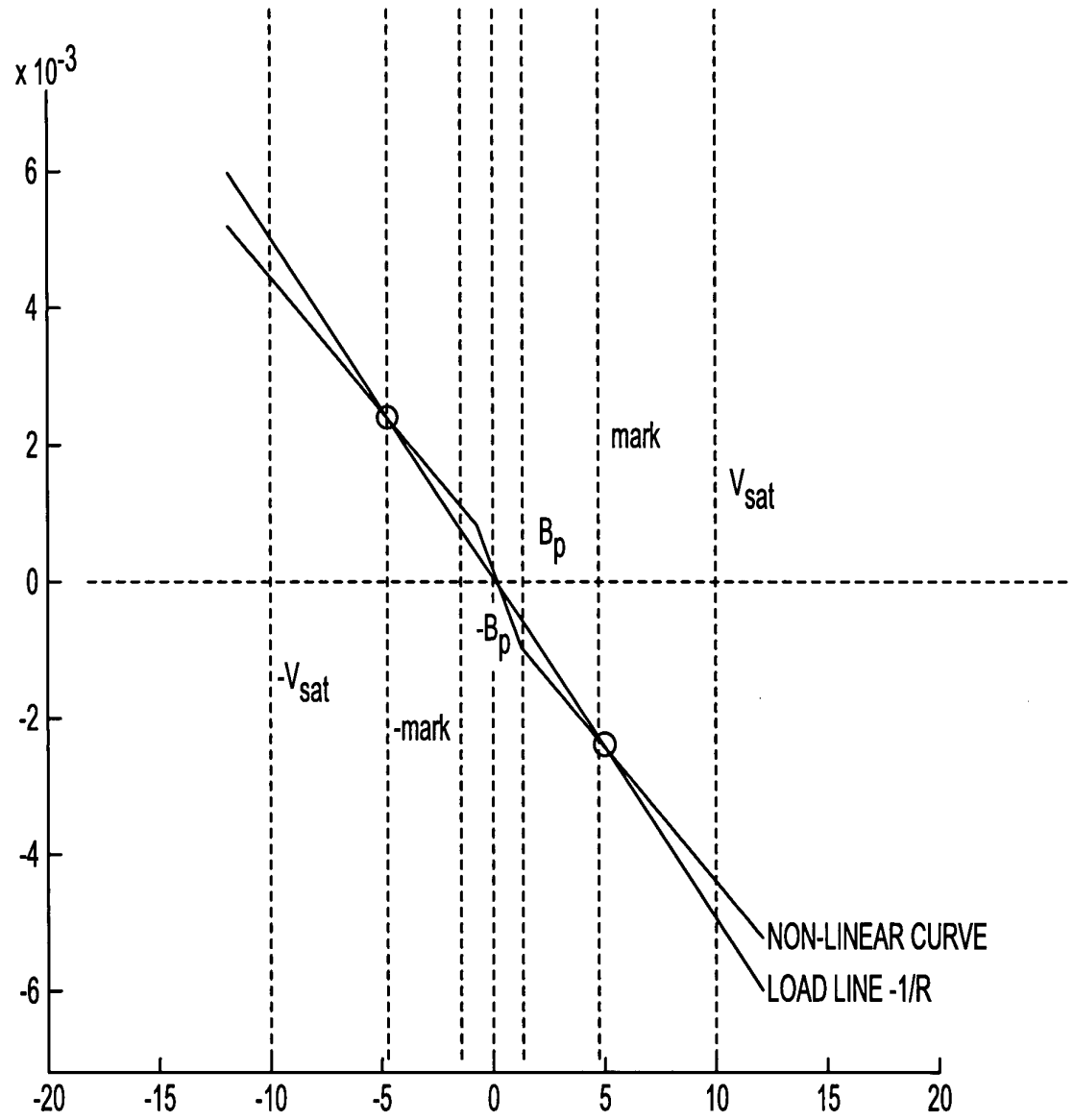

x 10^-3
6
4
2
0
-2
-4
-6
-20
-15
-10
-5
0
5
10
15
20
mark
V_sat
B_p
-B_p
-V_sat
-mark
NON-LINEAR CURVE
LOAD LINE -1/R

FIG. 21A

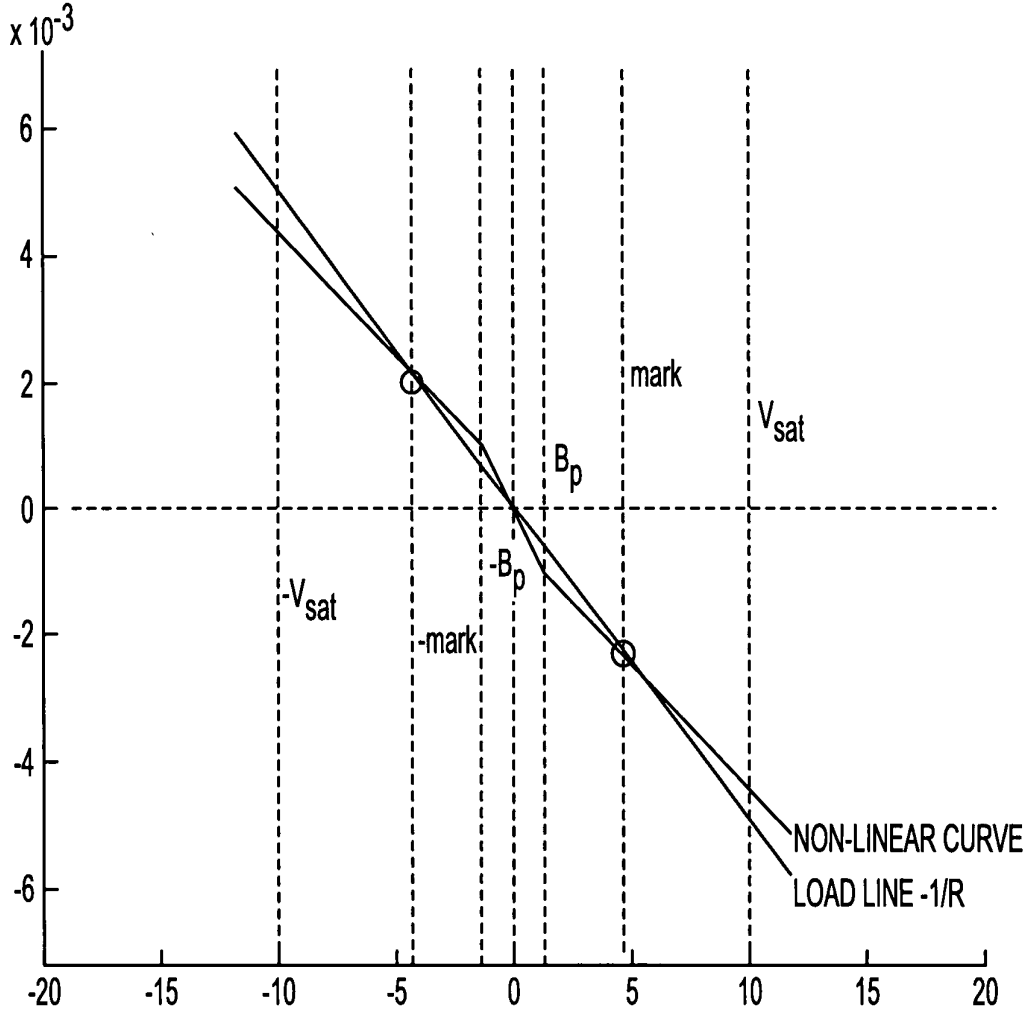

x 10-3
6
4
2
0
-2
-4
-6
-20
-15
-10
-5
0
5
10
15
20
mark
Vsat
Bp
-Bp
-Vsat
-mark
NON-LINEAR CURVE
LOAD LINE -1/R

FIG. 21B

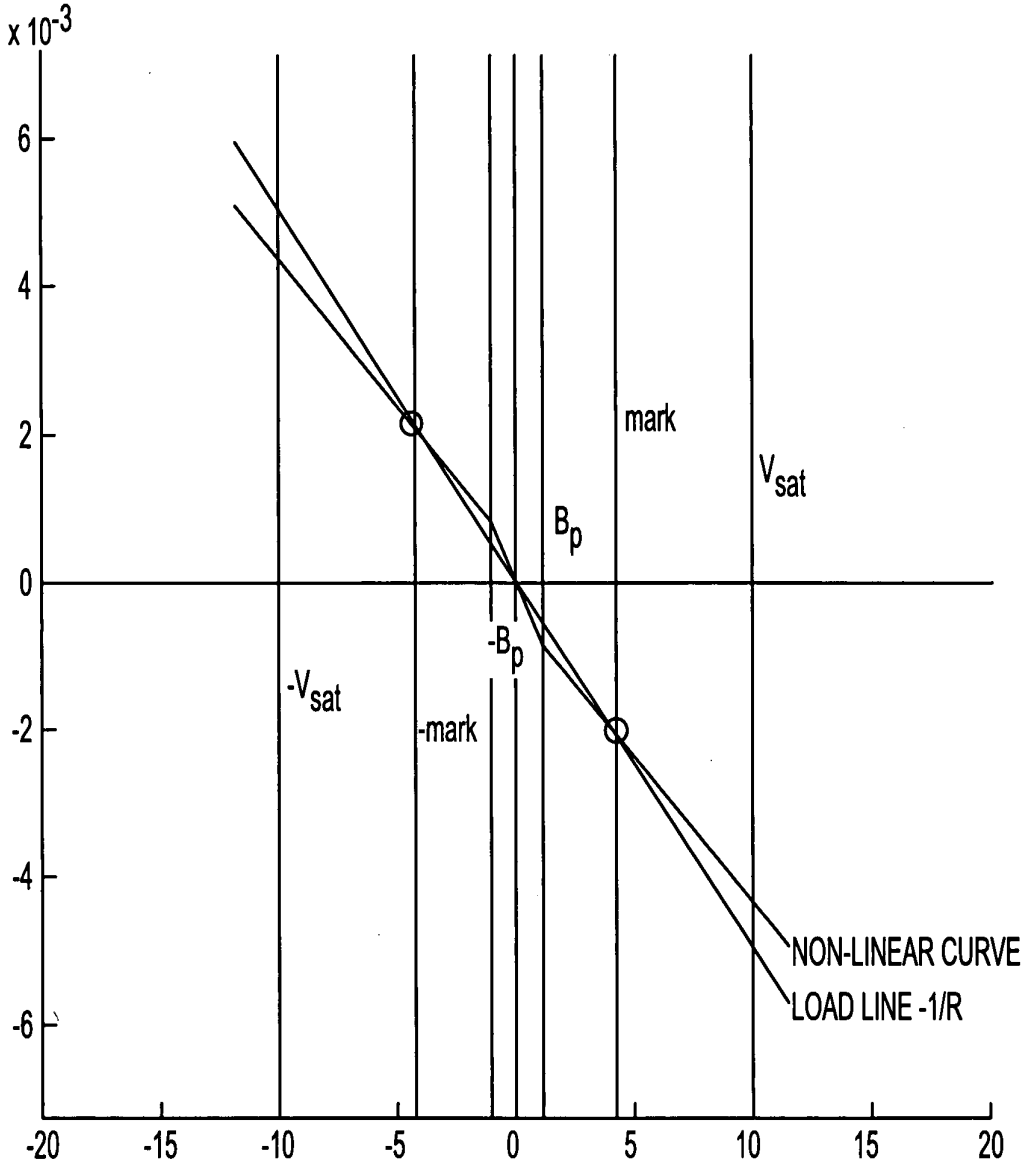

x 10-3
6
4
2
0
-2
-4
-6
-20
-15
-10
-5
0
5
10
15
20
mark
Vsat
Bp
-Bp
-Vsat
-mark
NON-LINEAR CURVE
LOAD LINE -1/R

FIG. 21C

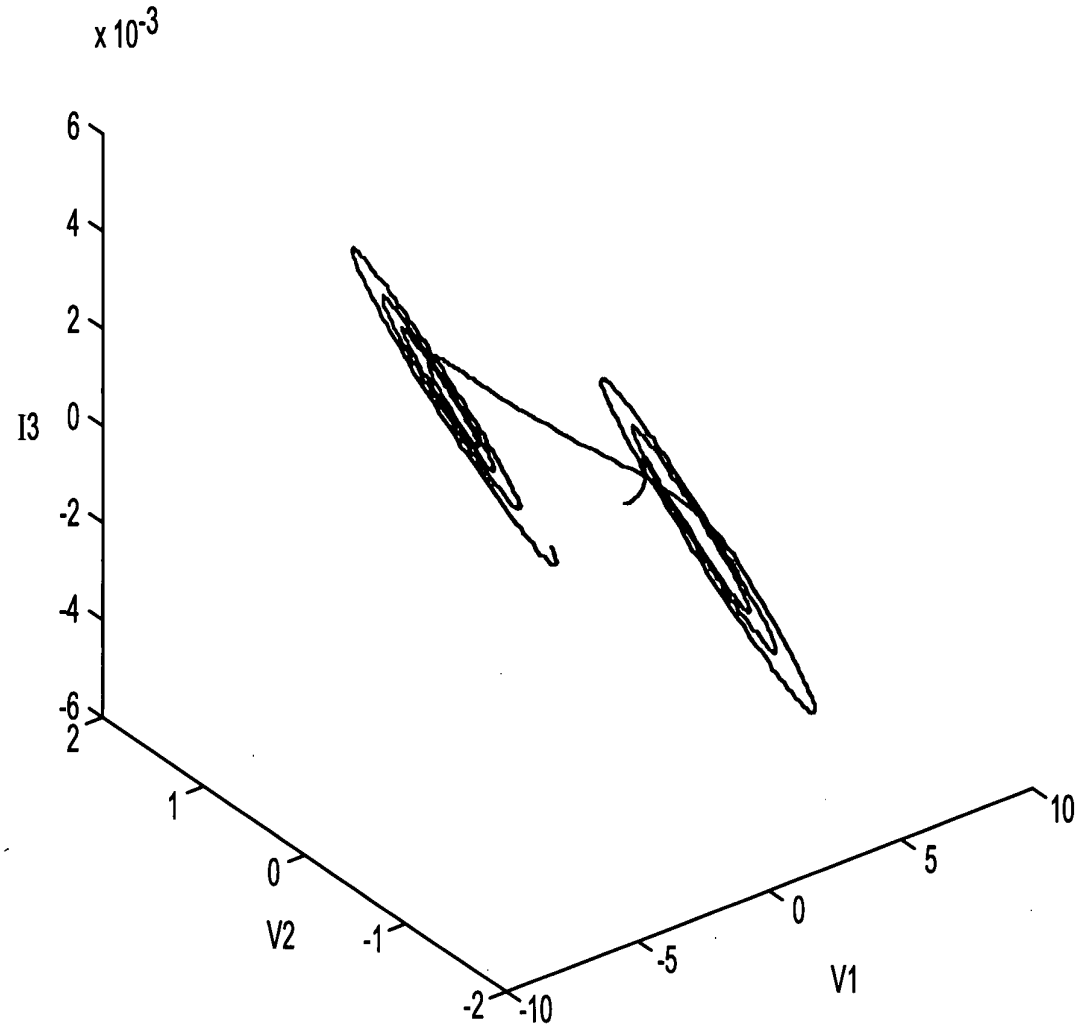


FIG. 21D

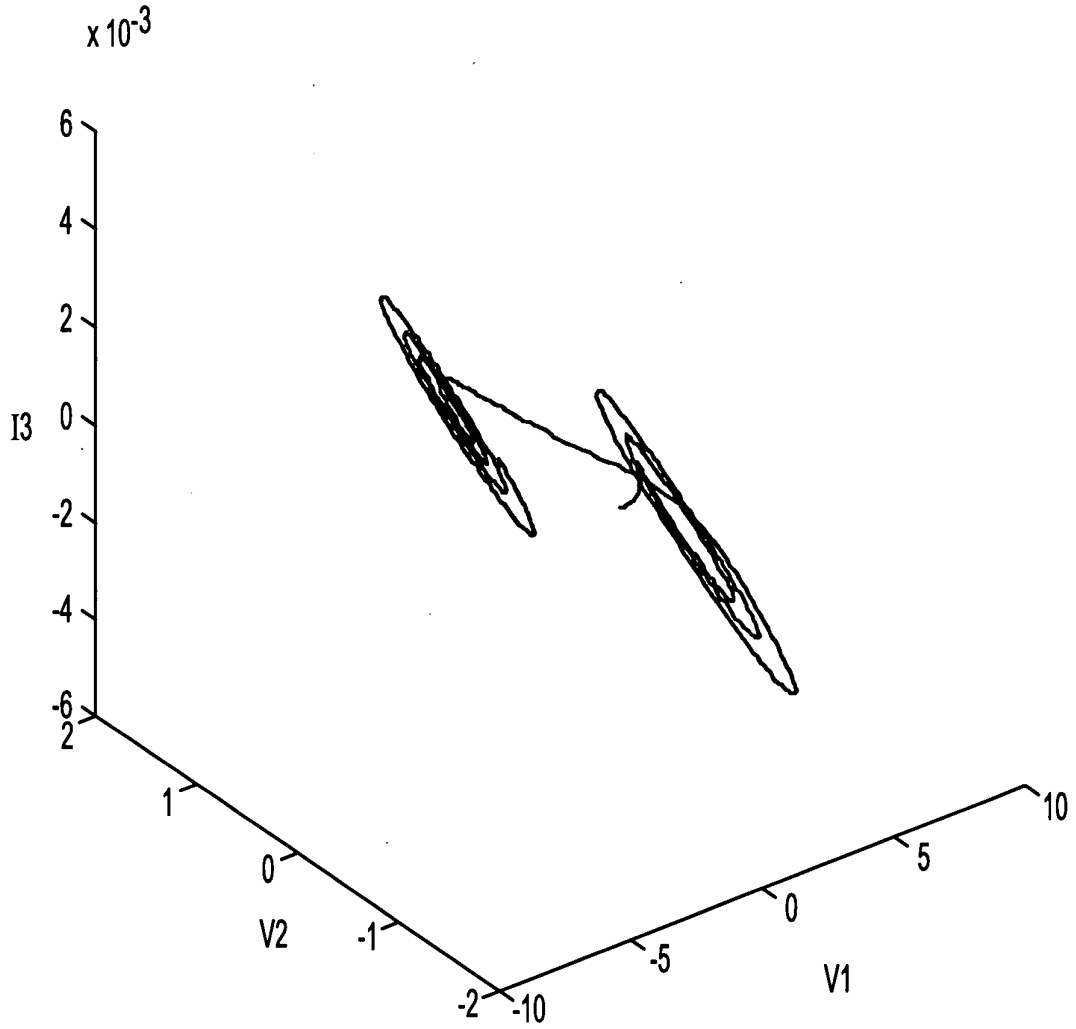


FIG. 21E

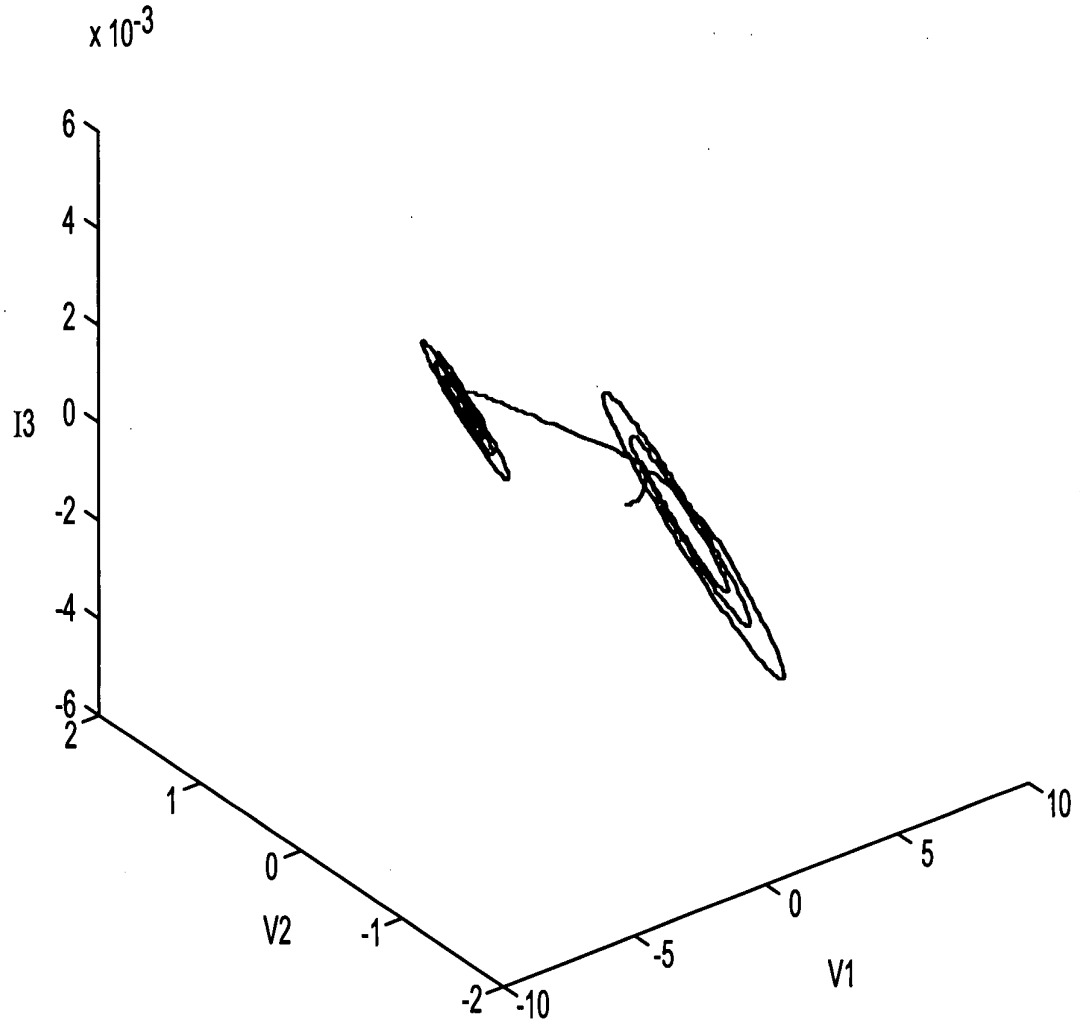


FIG. 21F

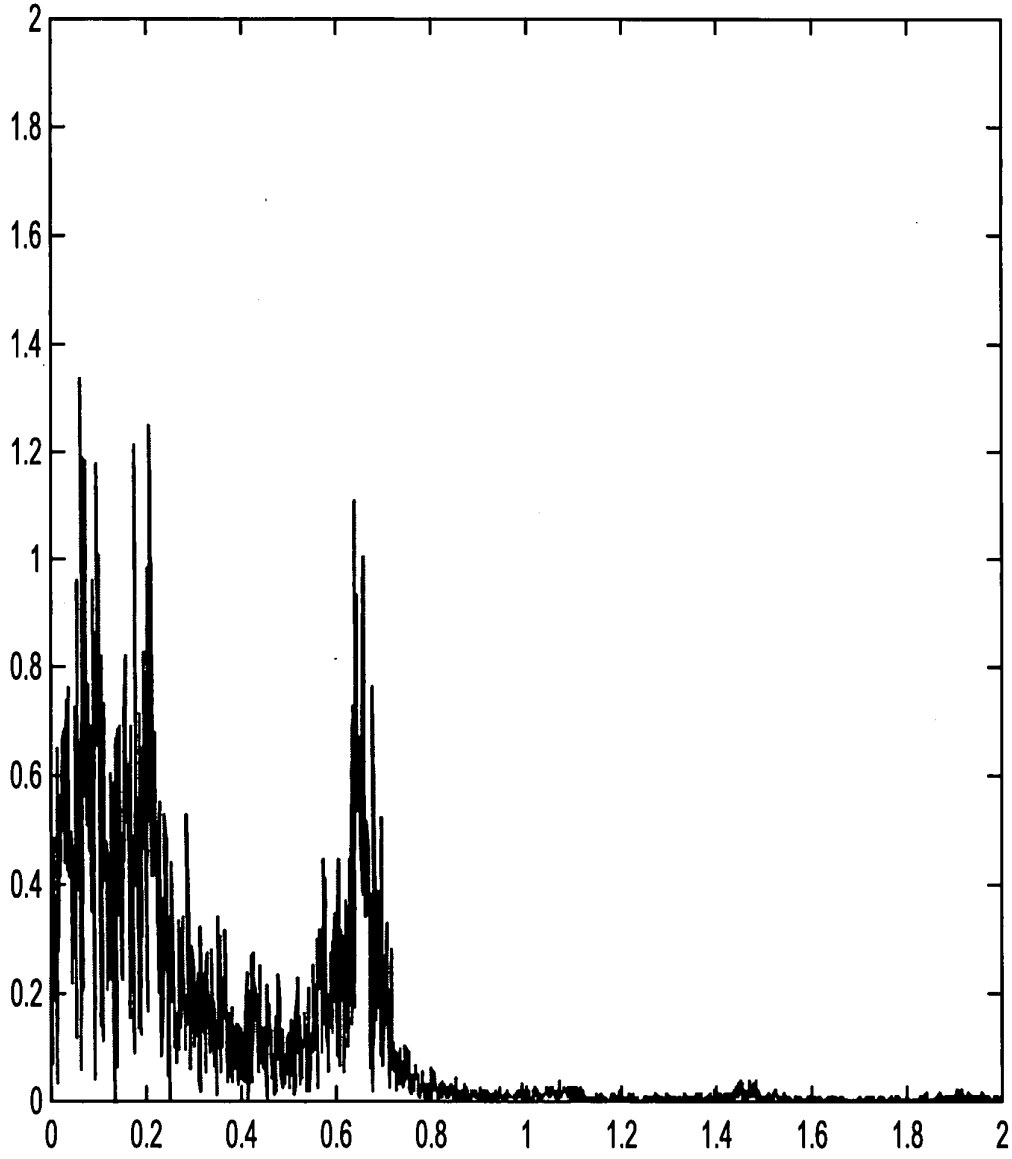


FIG. 21G

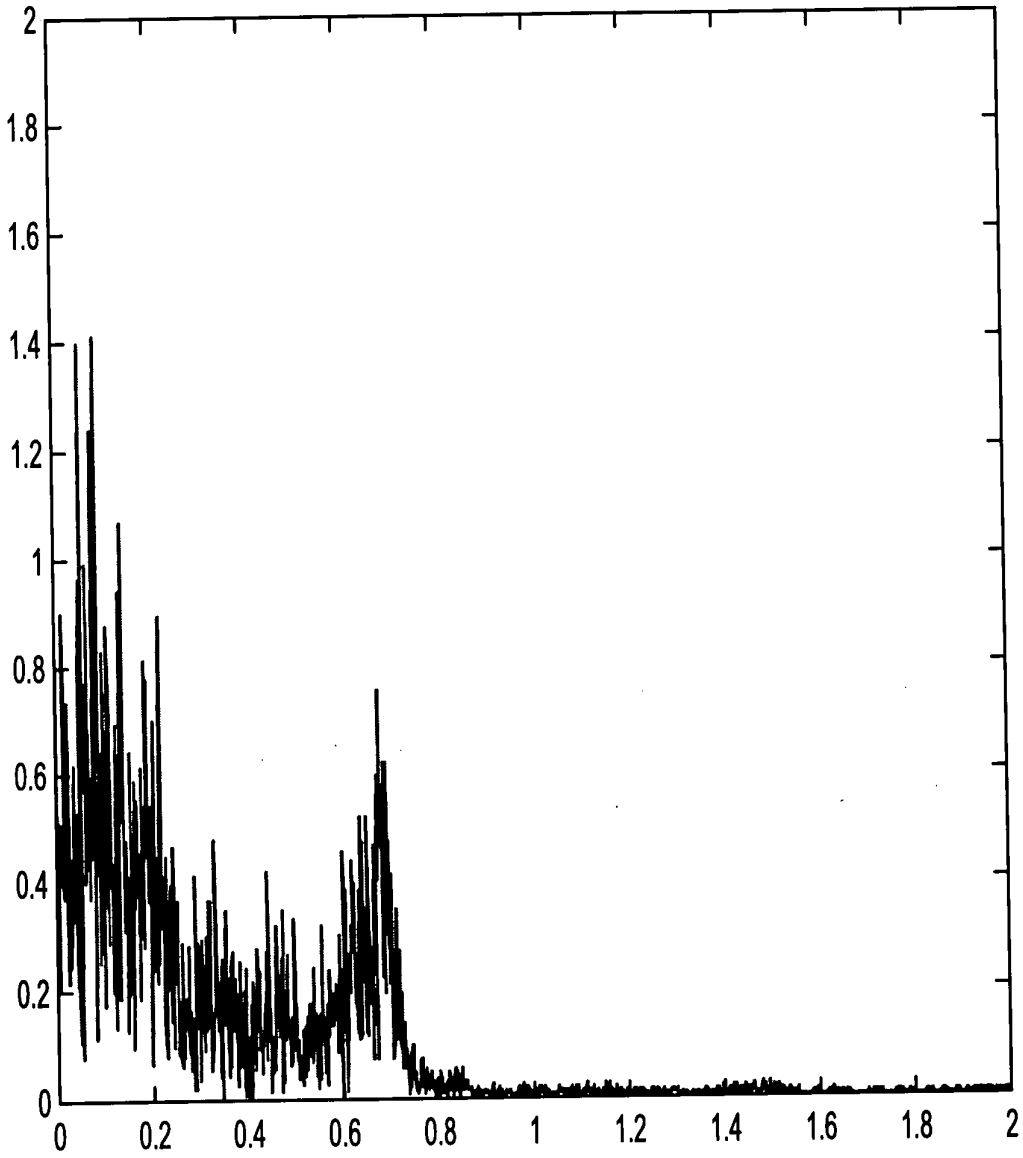


FIG. 21H

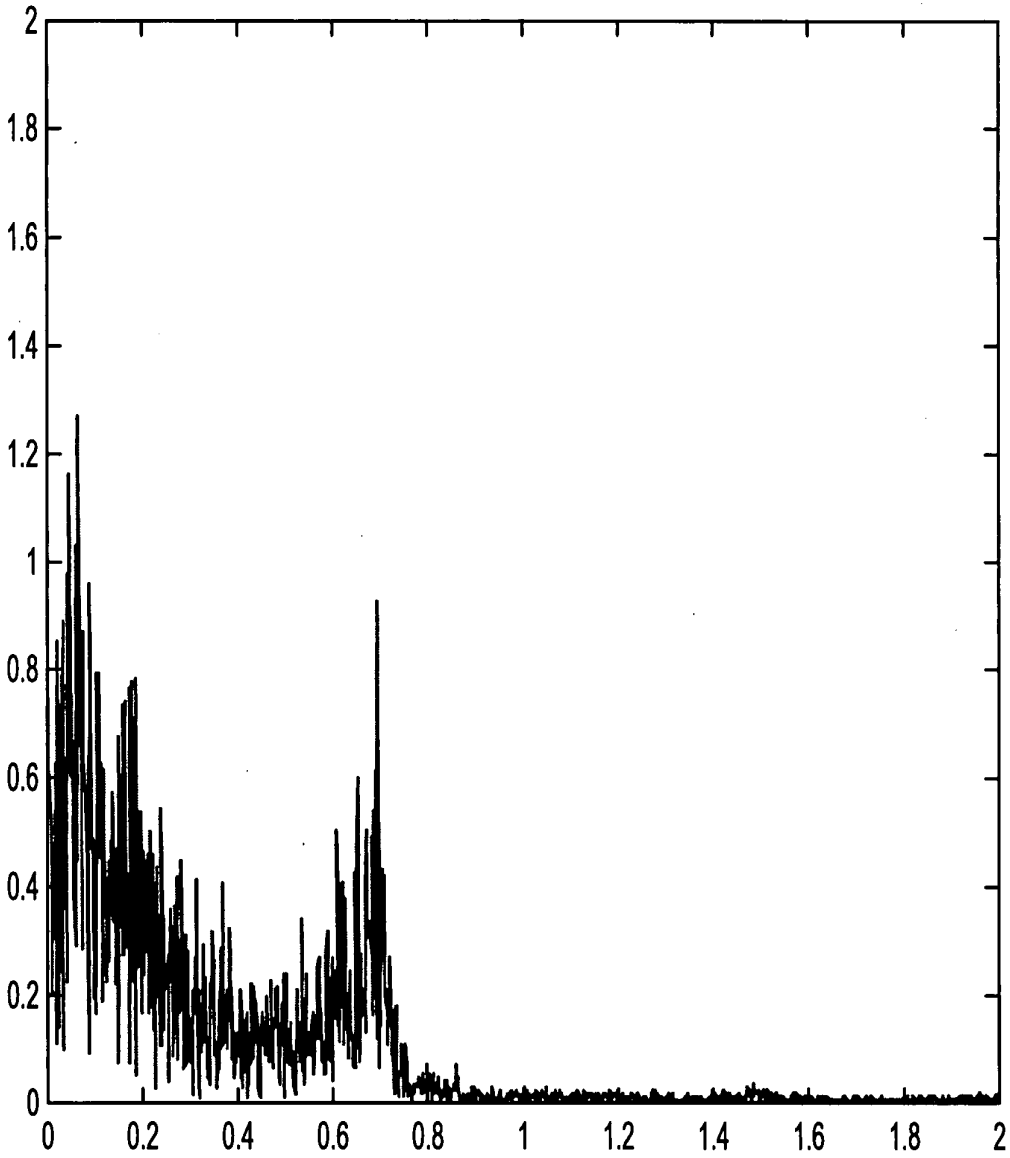


FIG. 21I

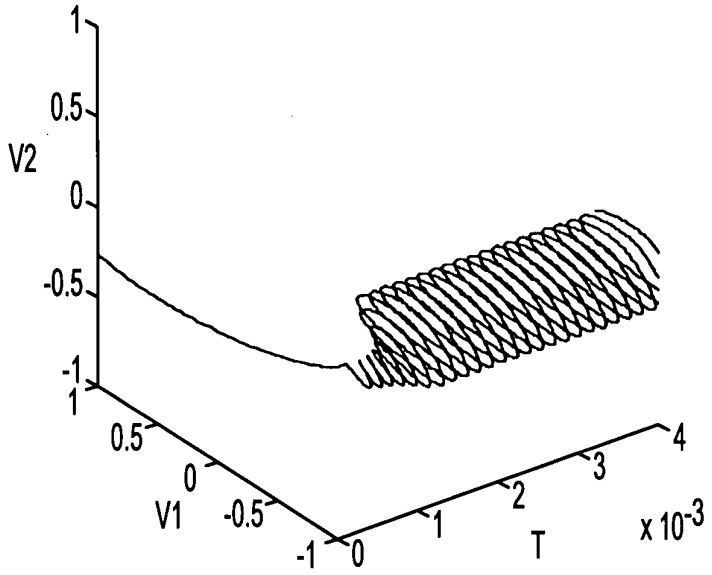


FIG. 22A

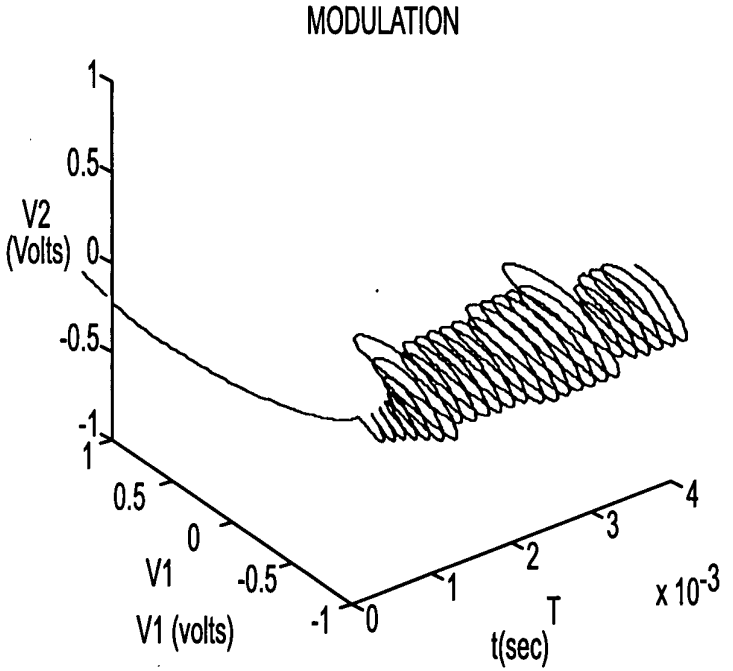


FIG. 22B

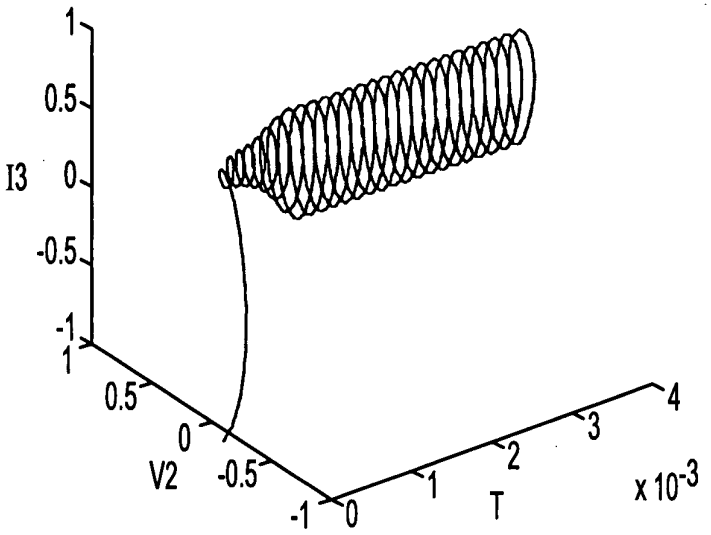


FIG. 22C

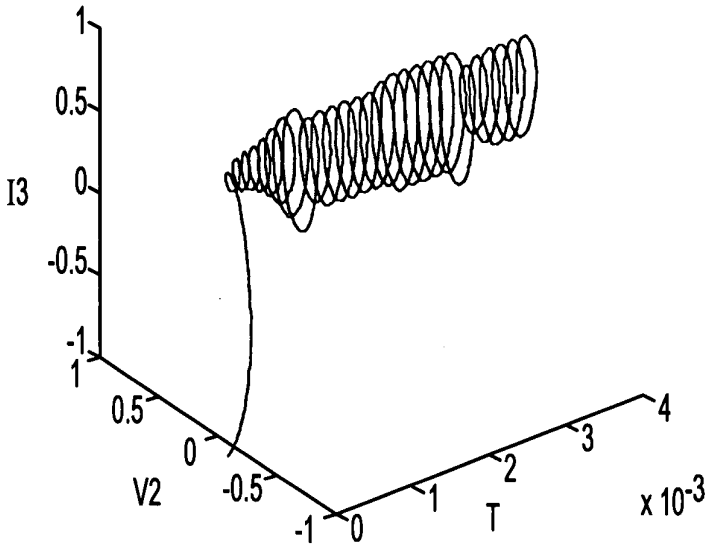


FIG. 22D

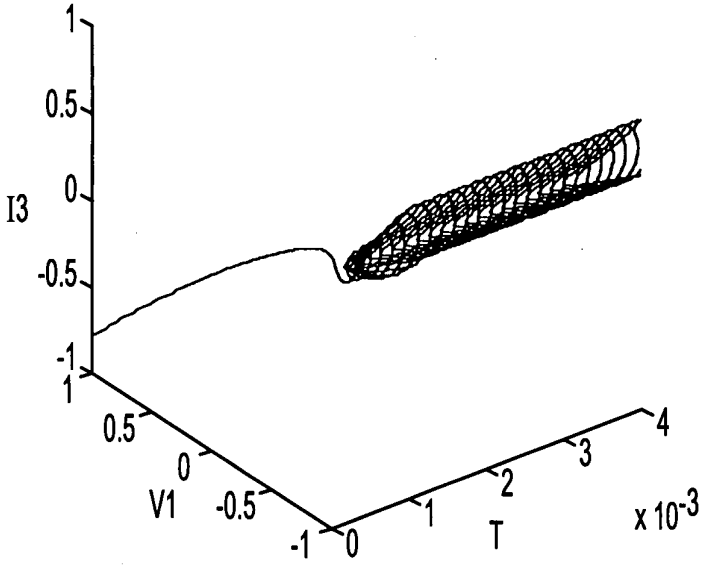


FIG. 22E

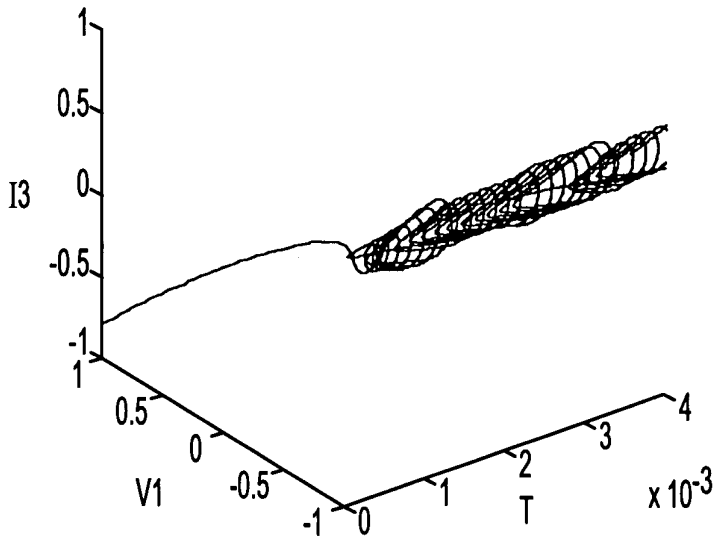
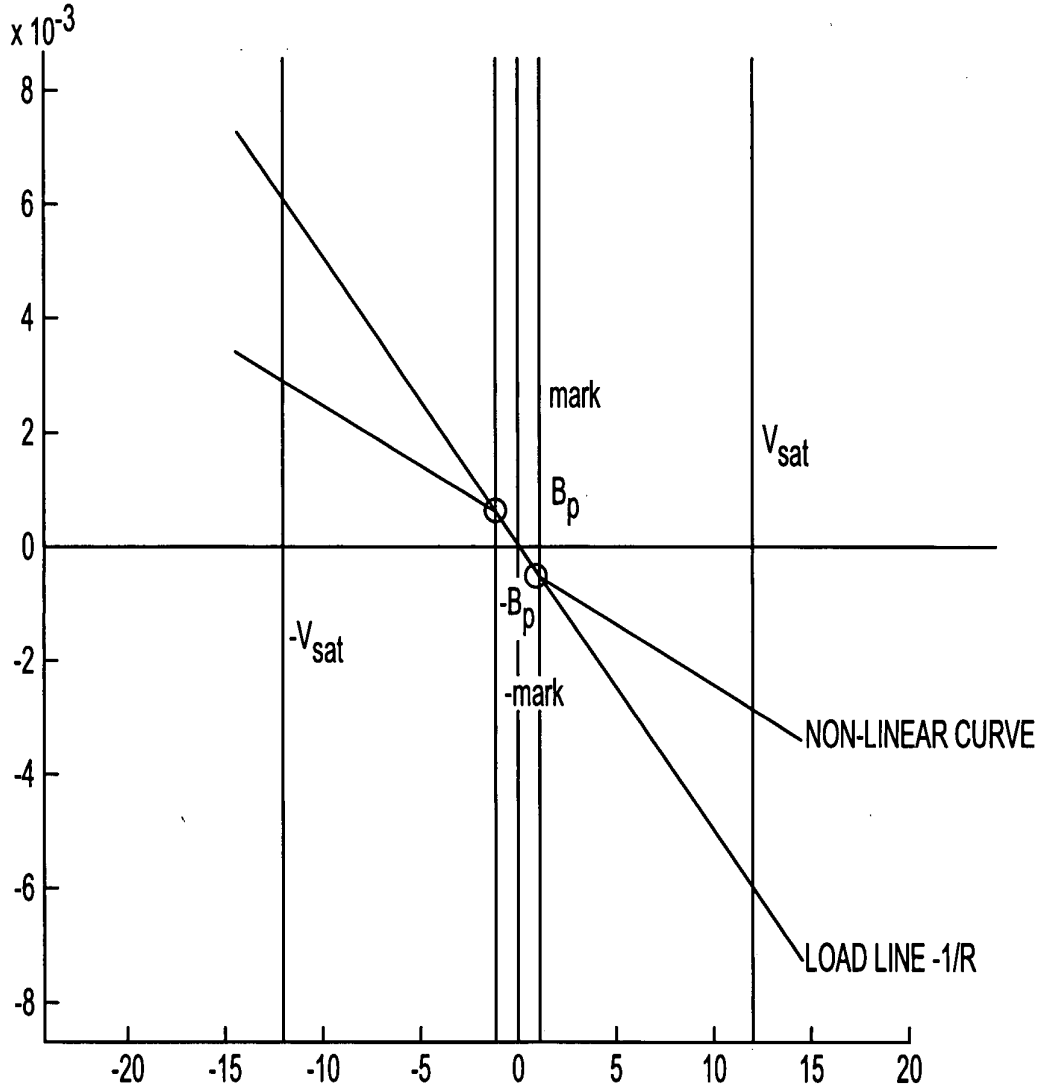


FIG. 22F


x 10-3
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6
4
2
0
-2
-4
-6
-8
-20
-15
-10
-5
0
5
10
15
20
mark
Vsat
Bp
-Bp
-Vsat
-mark
NON-LINEAR CURVE
LOAD LINE -1/R

FIG. 23A

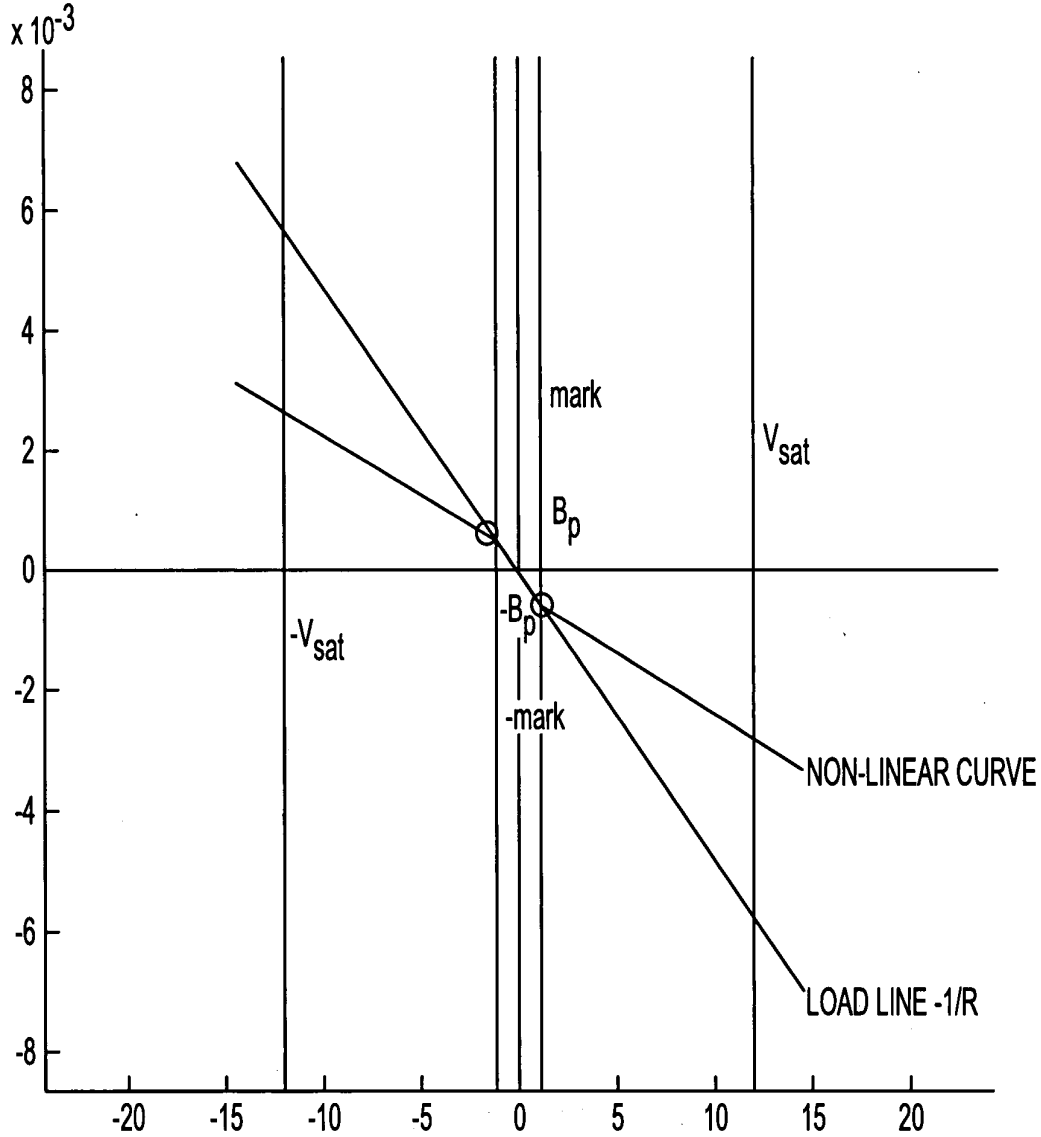

x 10-3
8
6
4
2
0
-2
-4
-6
-8
-20
-15
-10
-5
0
5
10
15
20
mark
Vsat
Bp
-Bp
-Vsat
-mark
NON-LINEAR CURVE
LOAD LINE -1/R

FIG. 23B

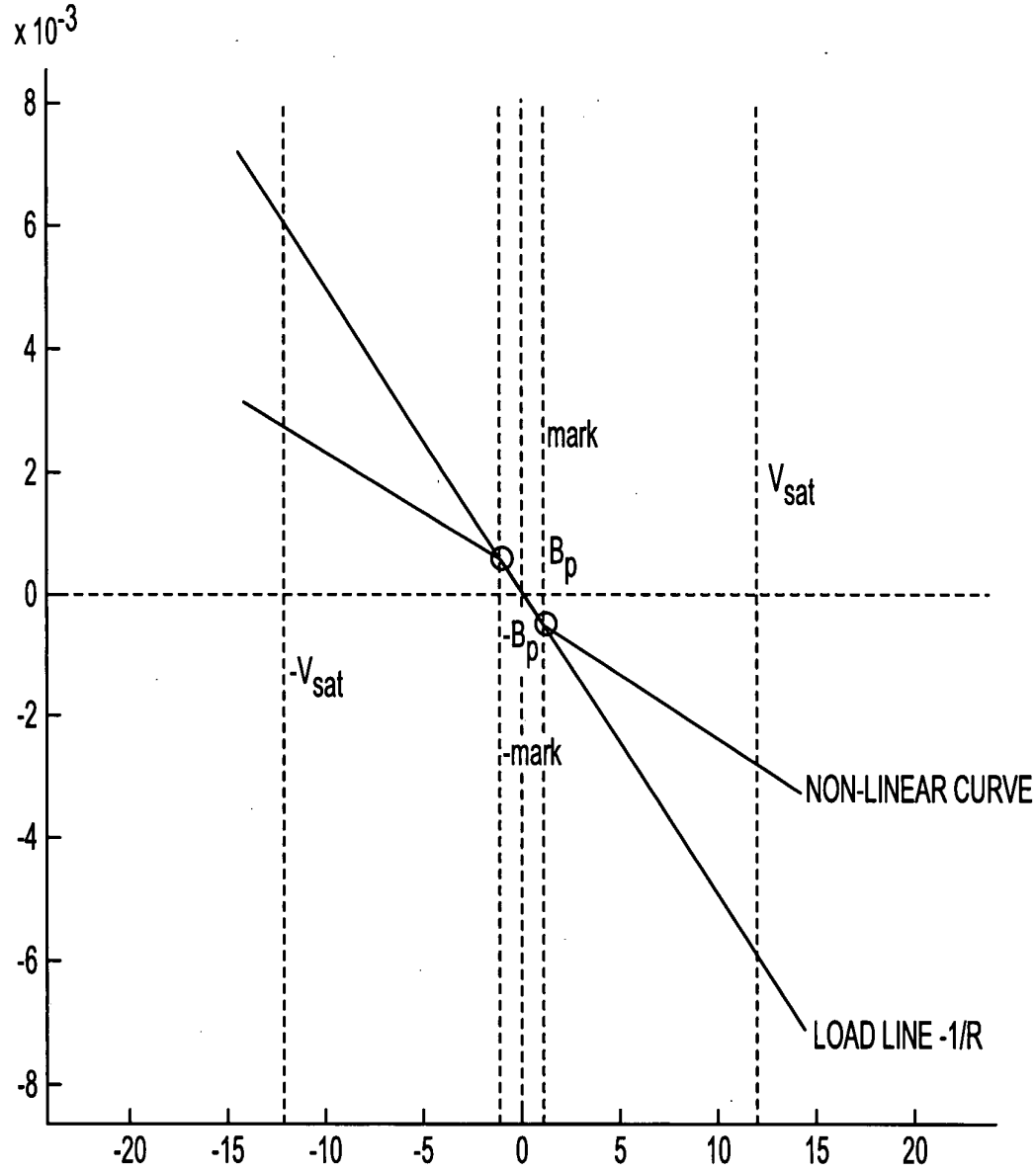

x 10-3
8
6
4
2
0
-2
-4
-6
-8
-20
-15
-10
-5
0
5
10
15
20
mark
Vsat
Bp
-Bp
-Vsat
-mark
NON-LINEAR CURVE
LOAD LINE -1/R

FIG. 23C

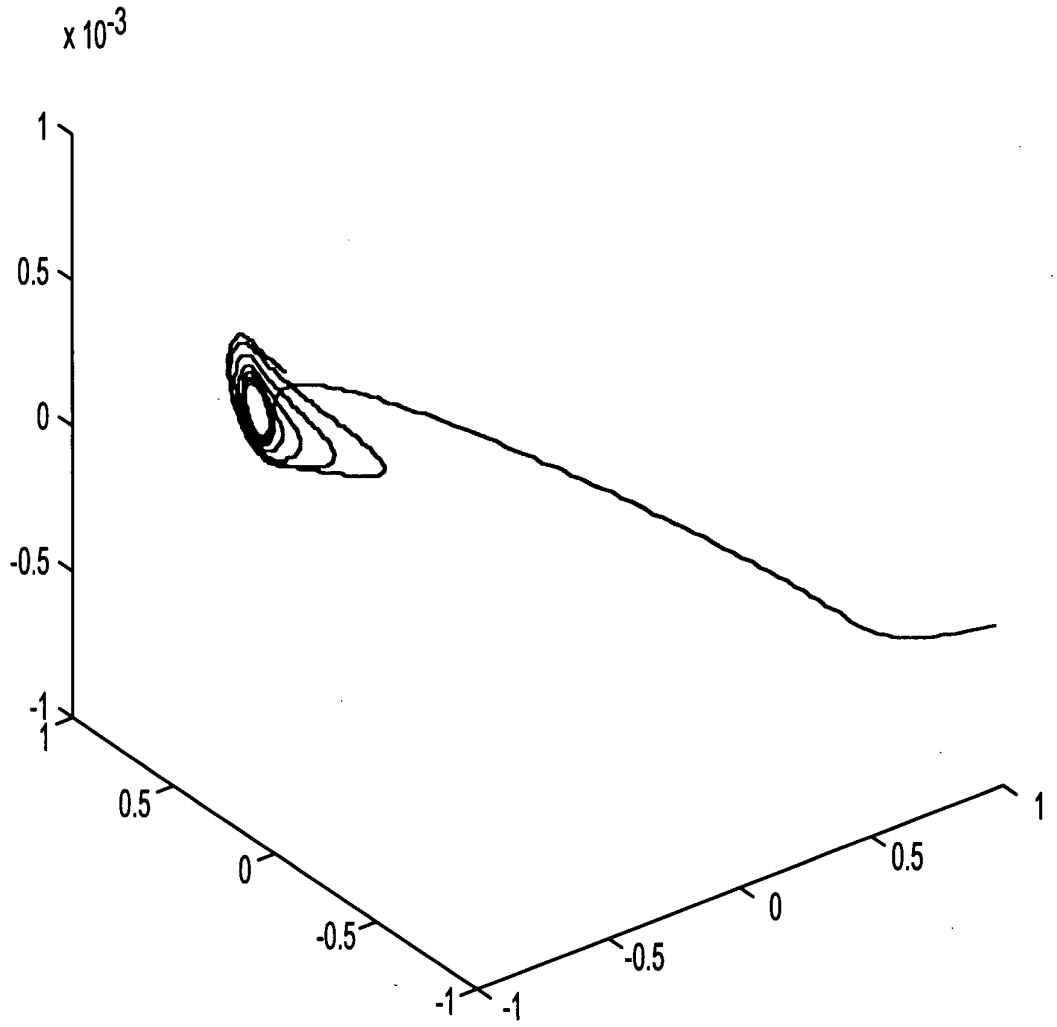


FIG. 23D

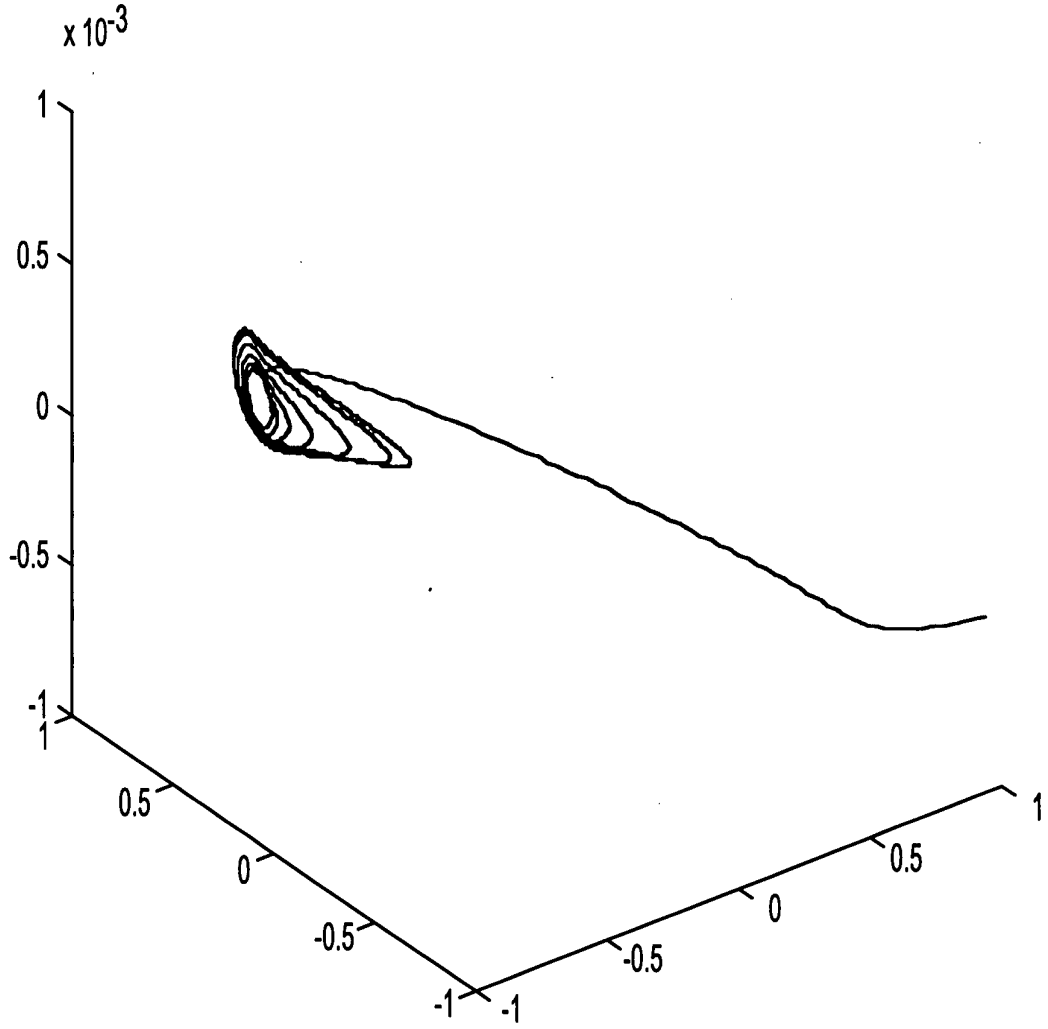


FIG. 23E

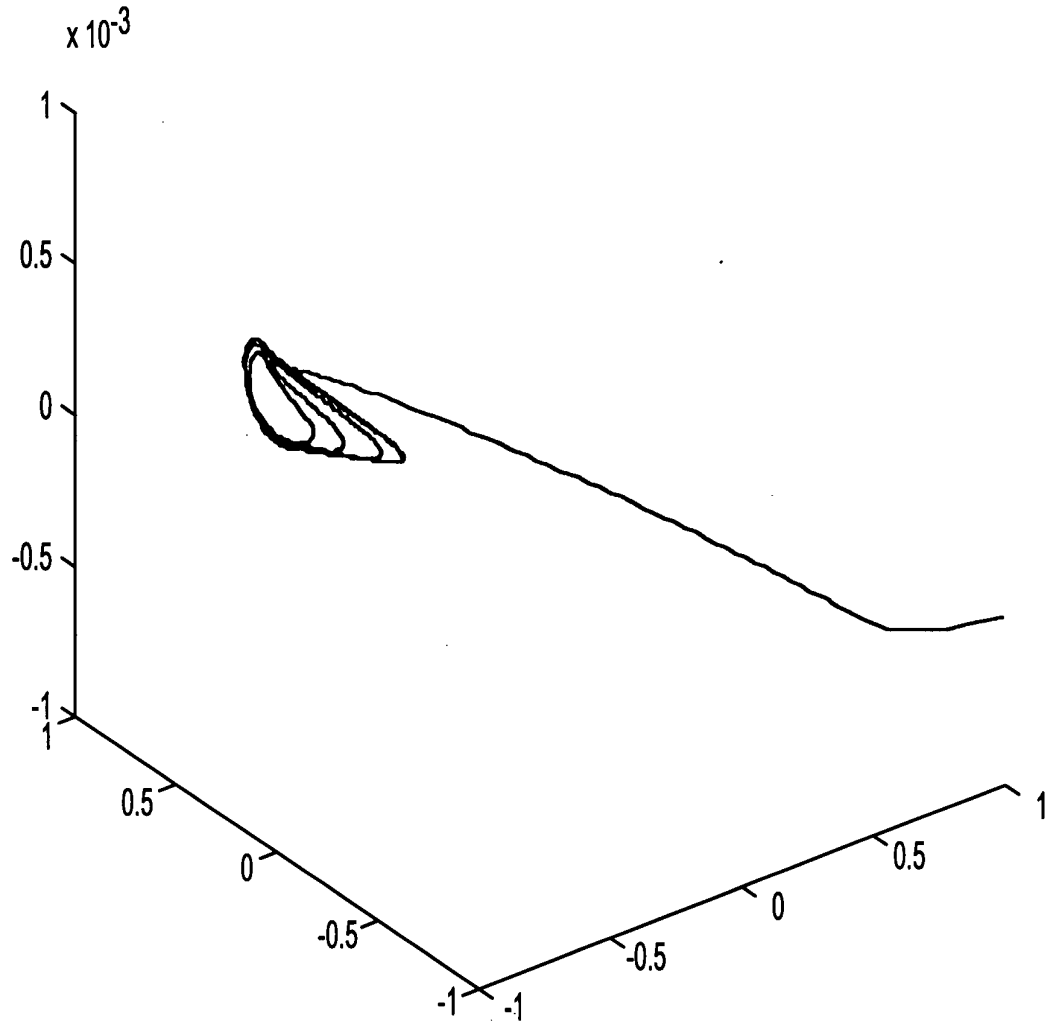
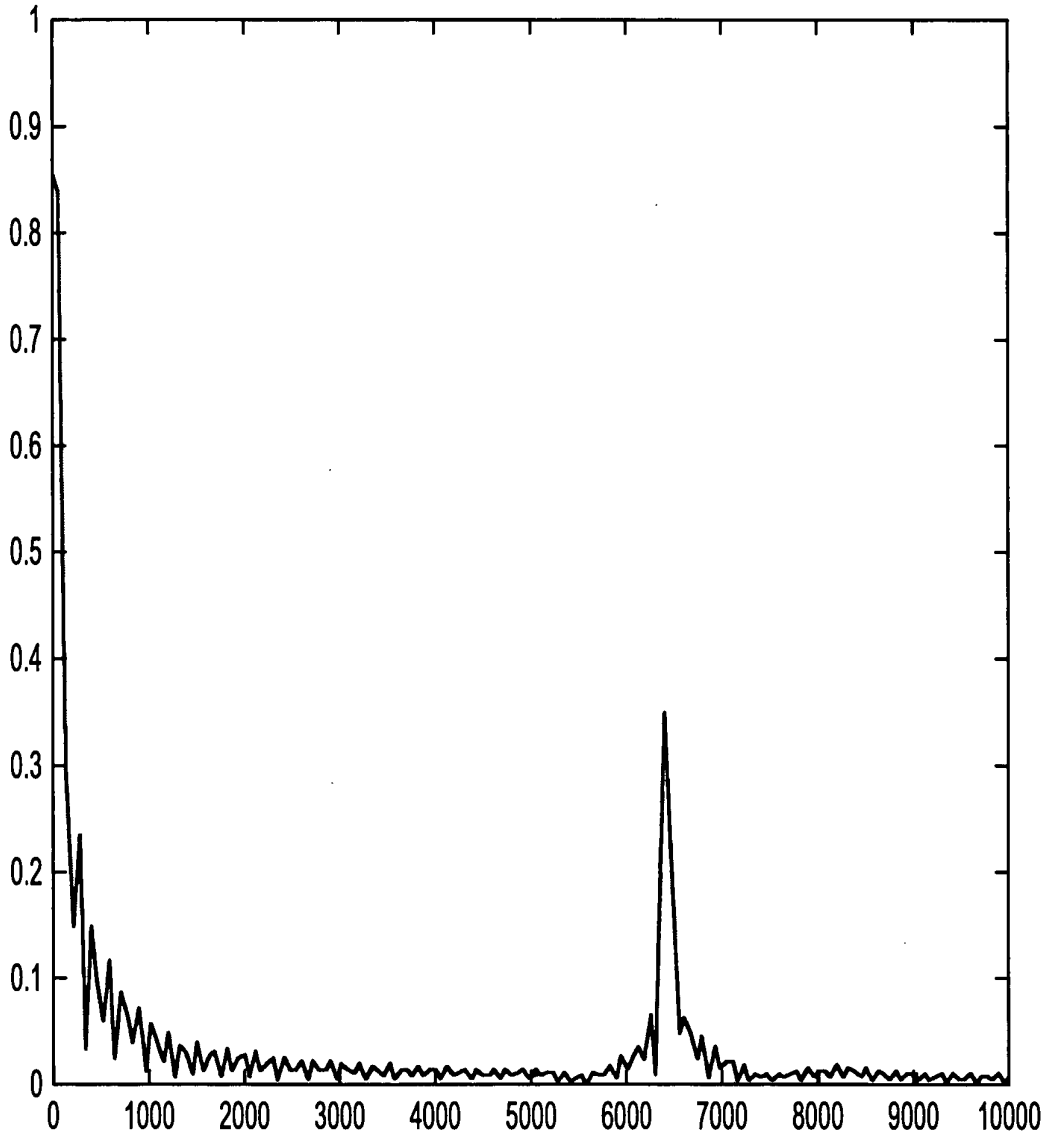


FIG. 23F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0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0
1000
2000
3000
4000
5000
6000
7000
8000
9000
10000

FIG. 23G

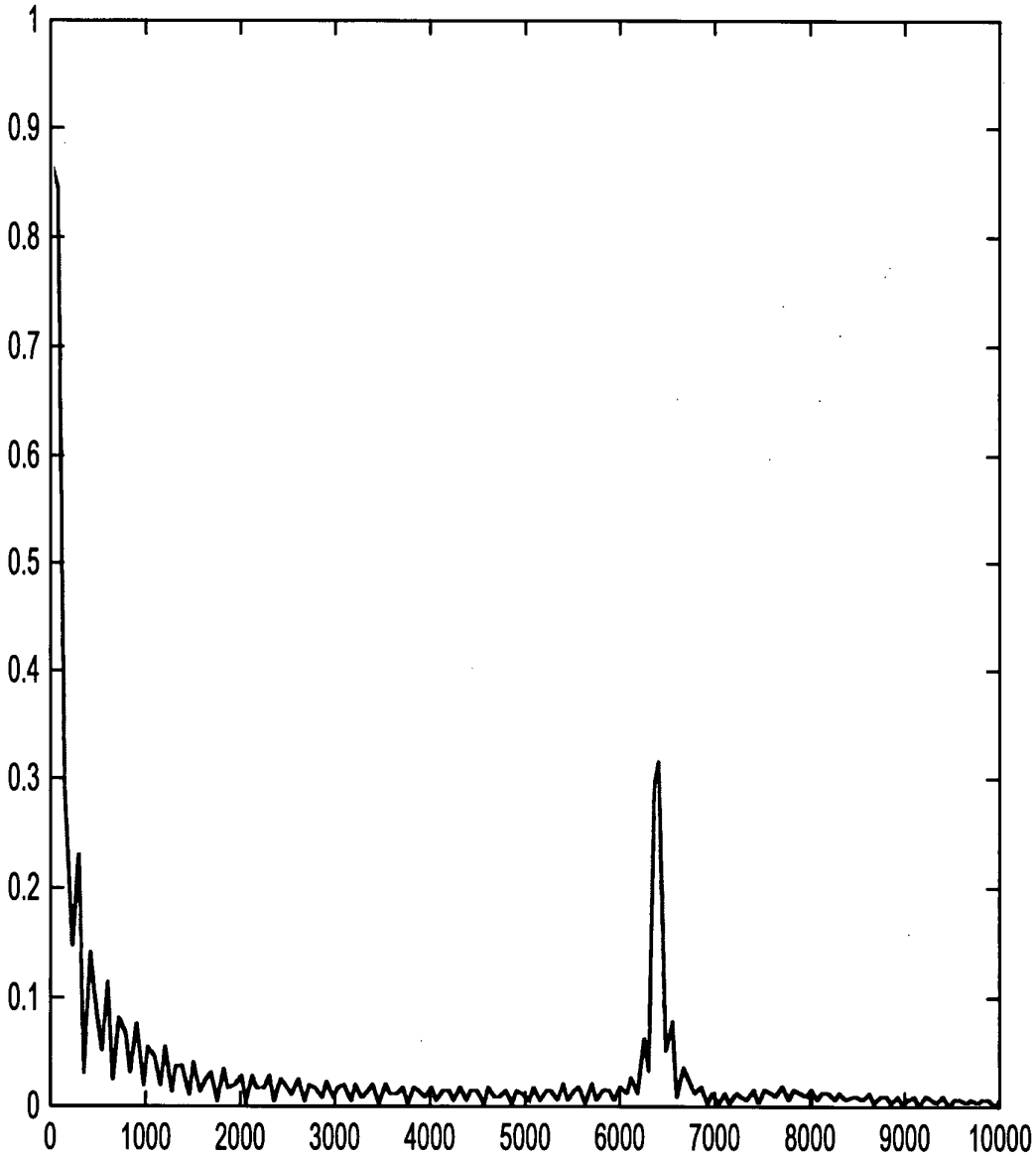

1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0
1000
2000
3000
4000
5000
6000
7000
8000
9000
10000

FIG. 23H

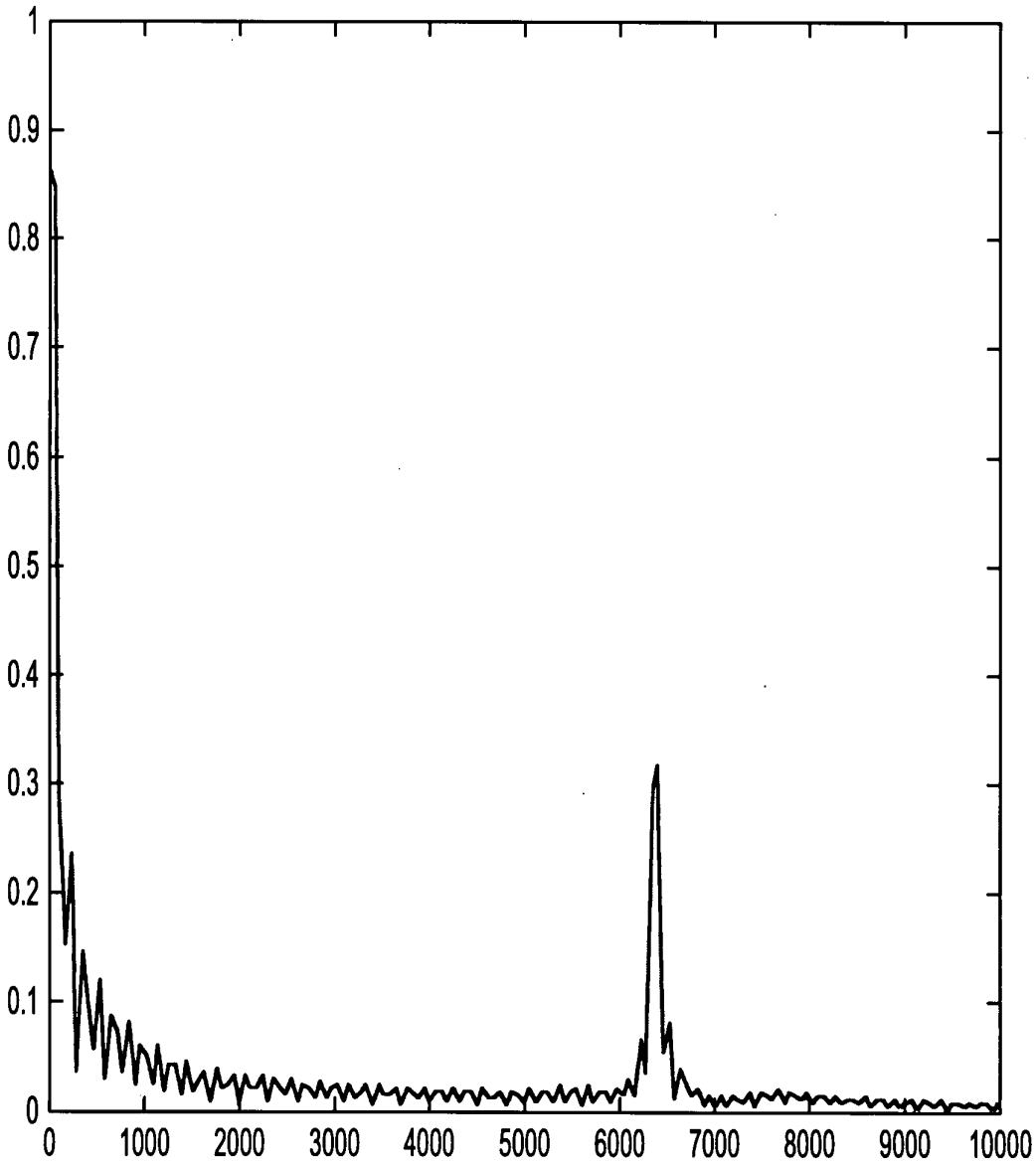

1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0
1000
2000
3000
4000
5000
6000
7000
8000
9000
10000

FIG. 23I

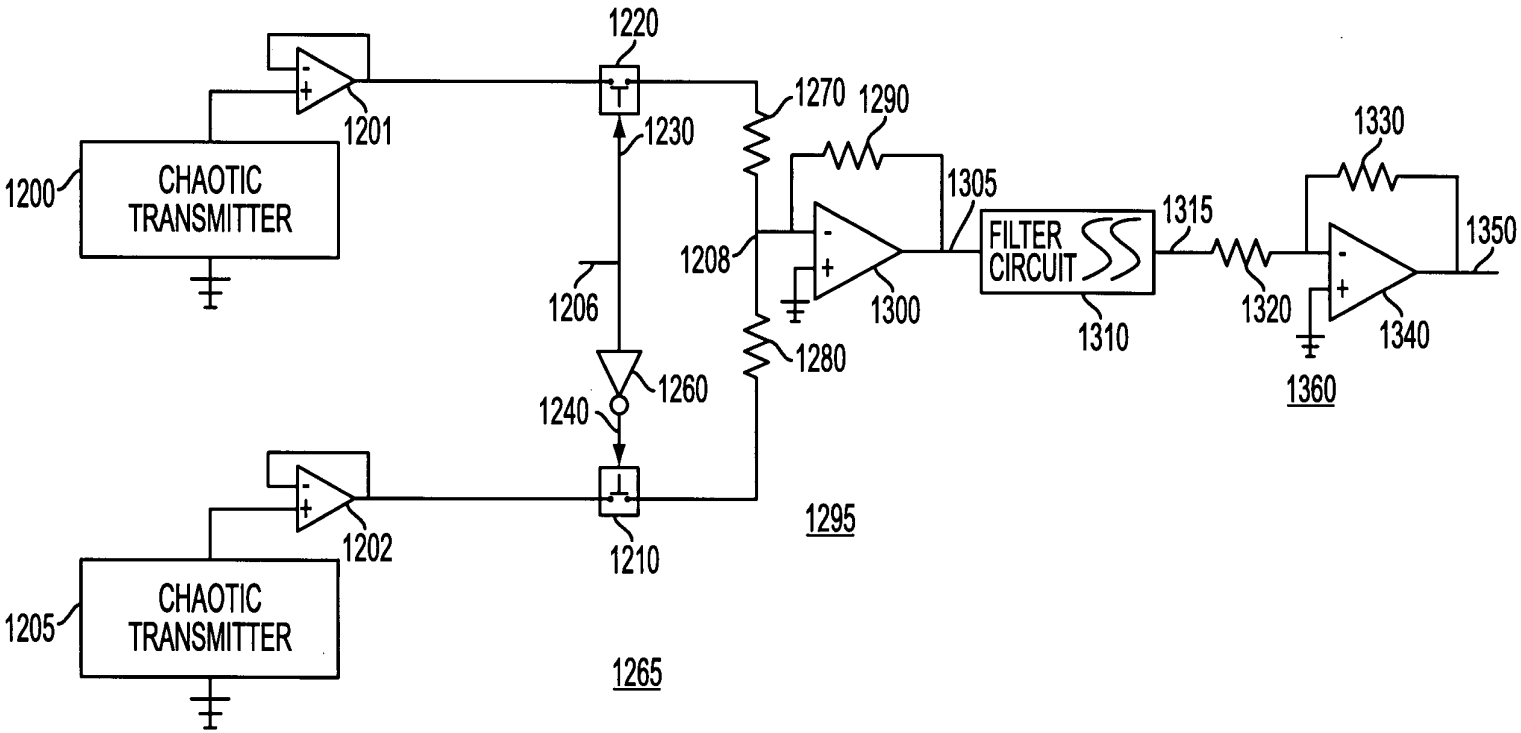

1220
1270
1290
1330
1201
1230
1305
1315
1350
1200
CHAOTIC
TRANSMITTER
1208
FILTER
CIRCUIT
1206
1300
1320
1340
1310
1280
1360
1260
1240
1295
1202
1210
1205
CHAOTIC
TRANSMITTER
1265

FIG. 24

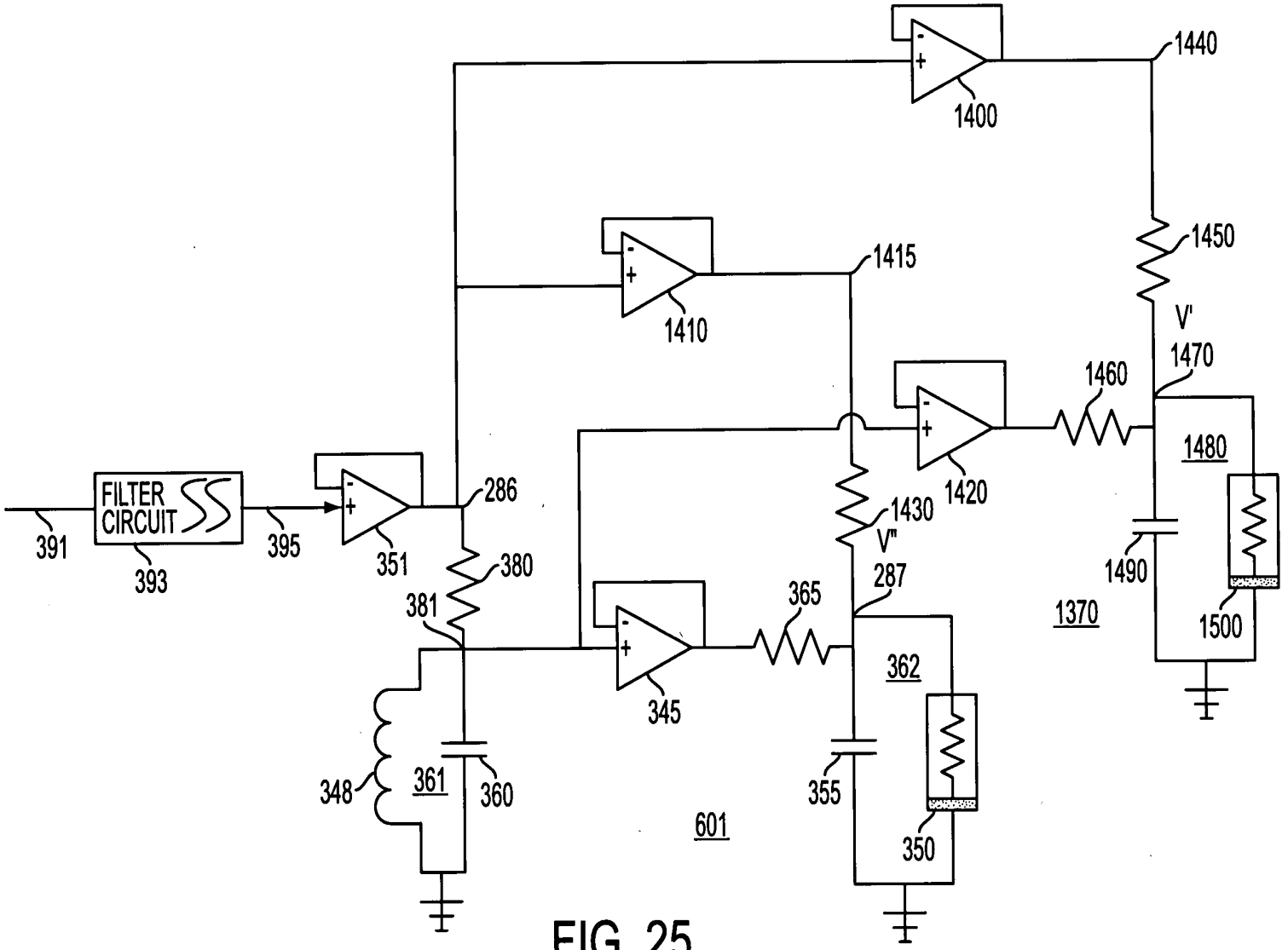

1440
1400
1450
1415
1410
V'
1470
1460
1480
1420
286
FILTER CIRCUIT
391
393
395
351
380
1430
V"
287
381
365
1490
1370
1500
362
345
348
361
360
355
601
350

FIG. 25

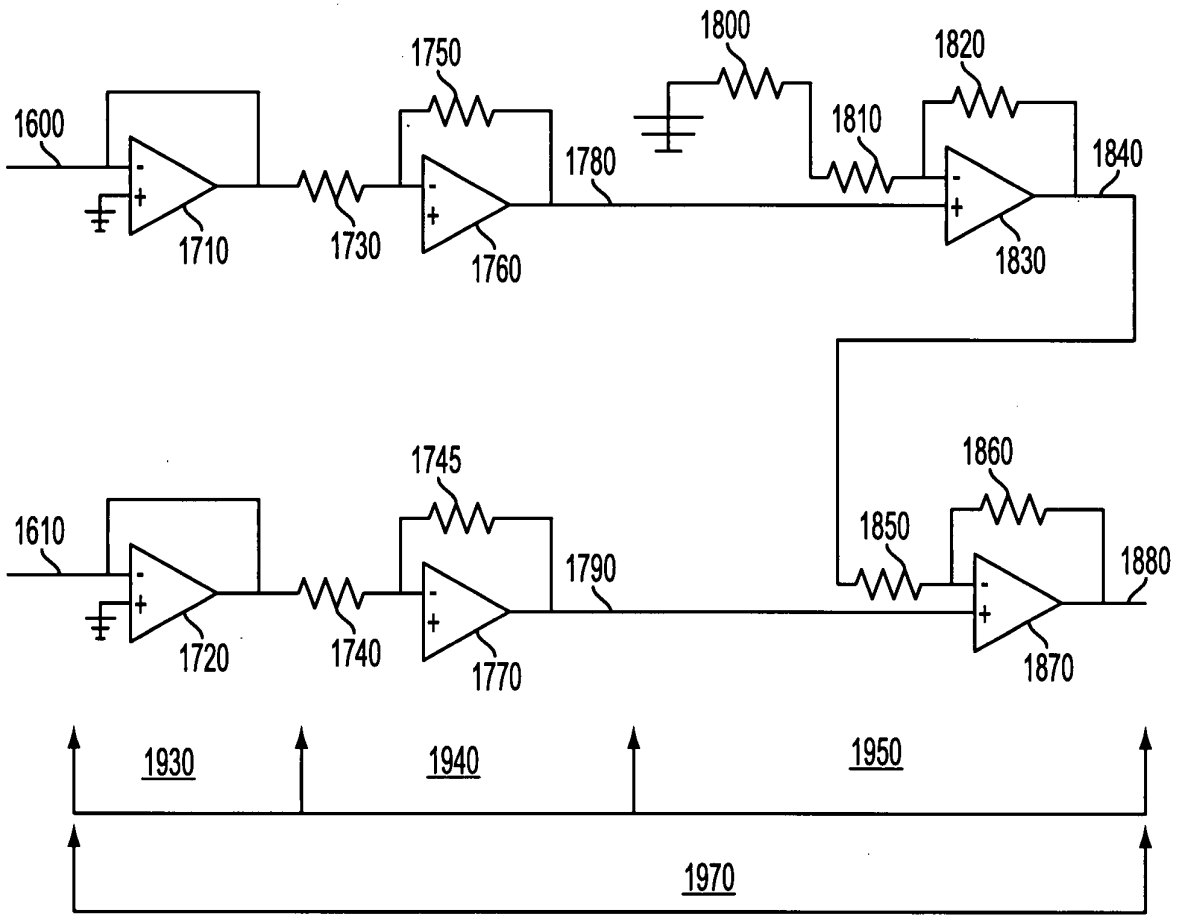
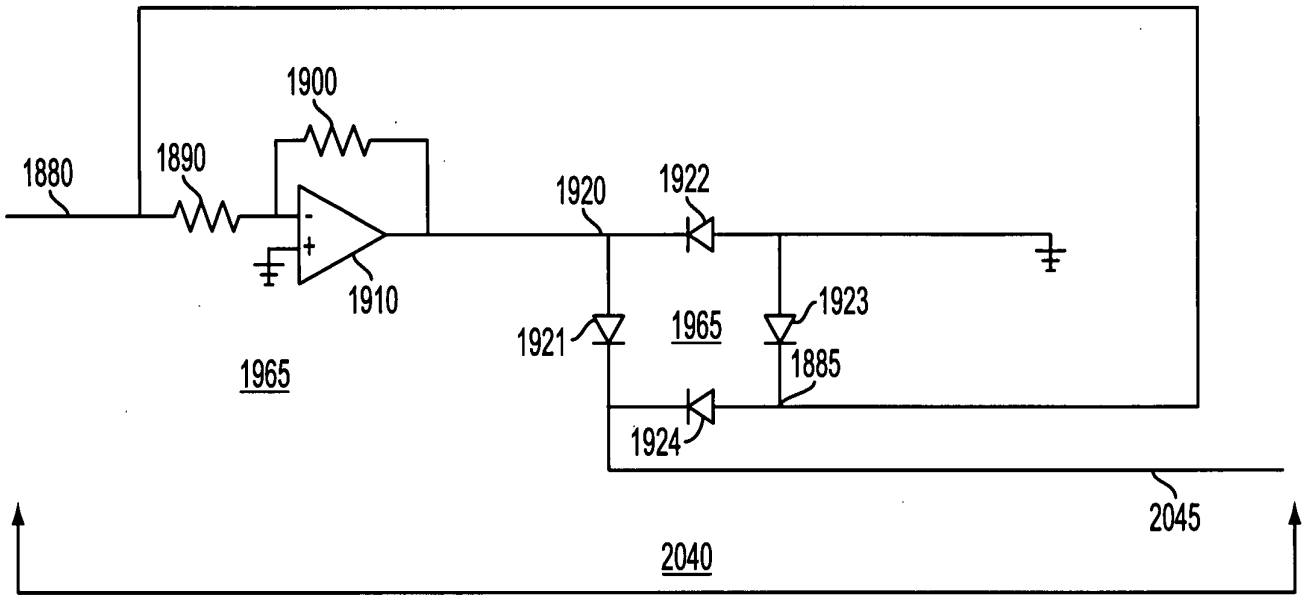

1600
1710
1730
1750
1760
1780
1800
1810
1820
1830
1840
1610
1720
1740
1745
1770
1790
1850
1860
1870
1880
1930
1940
1950
1970

FIG. 26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1880
1890
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1922
1910
1923
1921
1965
1885
1965
1924
2045
2040

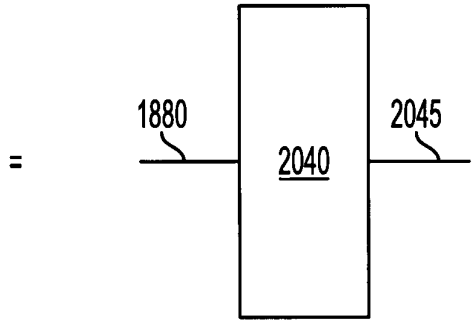
=
1880
2040
2045

FIG. 27

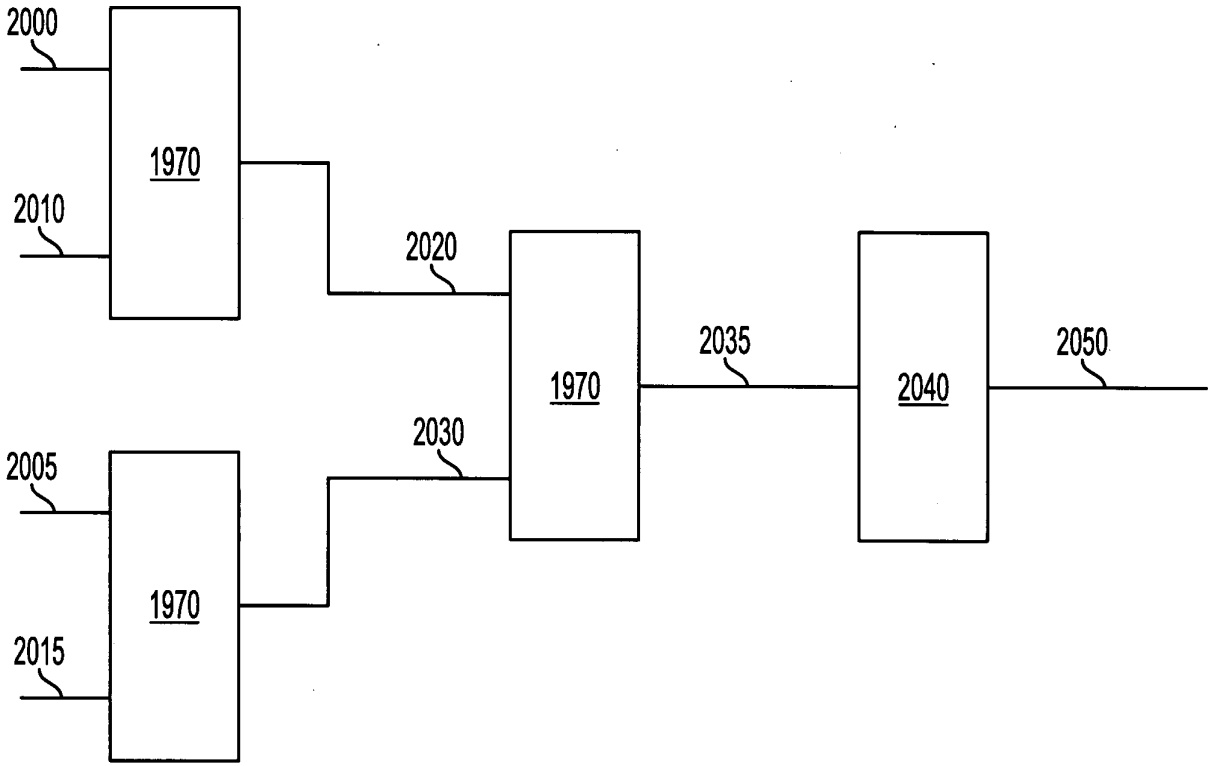

FIG. 28

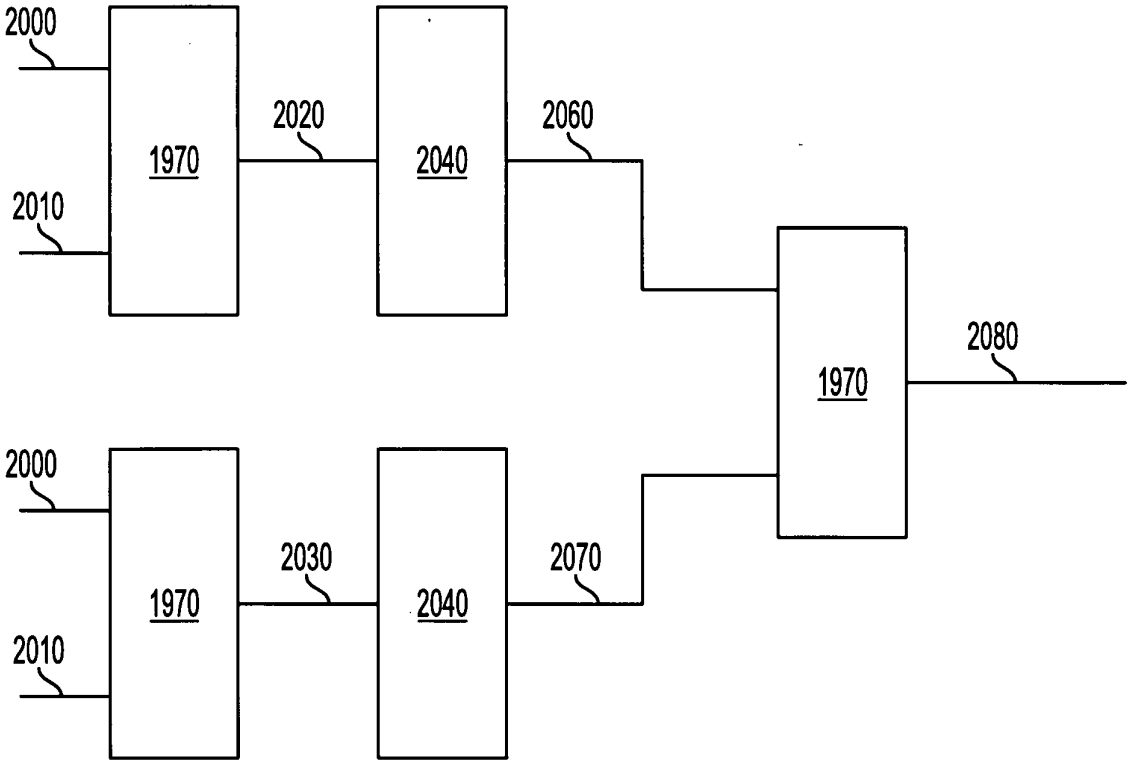
2000
2010
1970
2020
2040
2060
1970
2080
2000
2010
1970
2030
2040
2070

FIG. 29

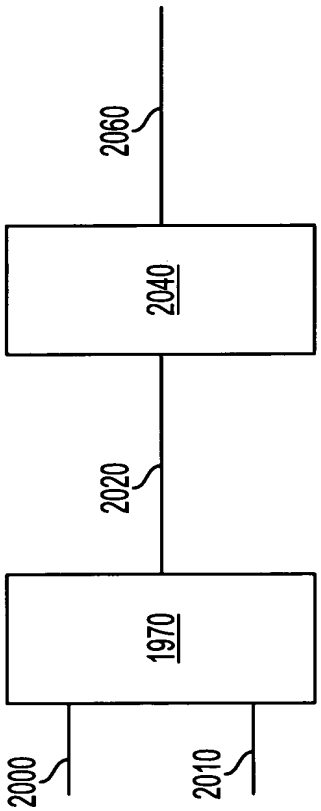

FIG. 30

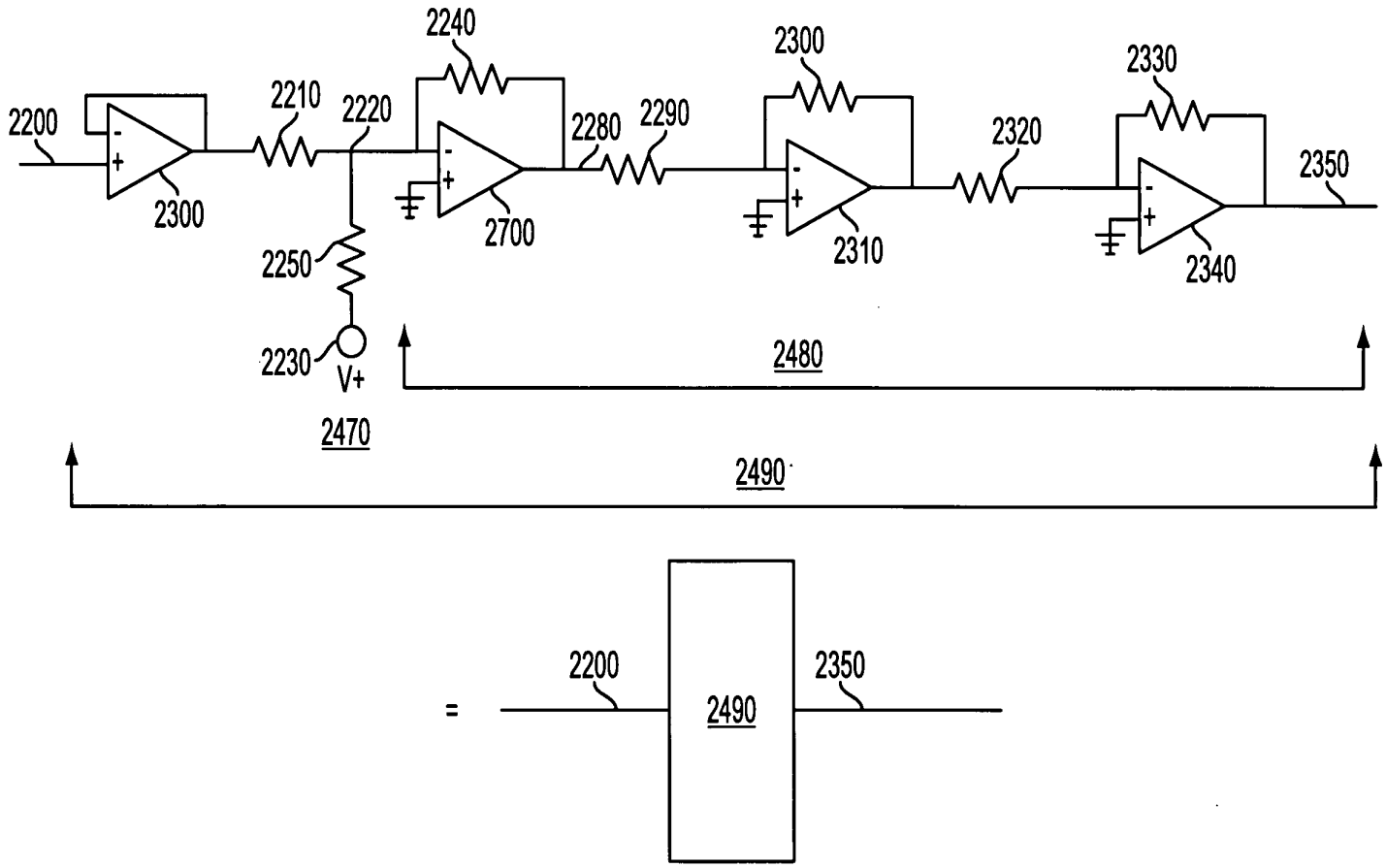
2200
2210
2220
2240
2280
2290
2300
2320
2330
2350
2250
2230
V+
2470
2480
2490
2700
2310
2340
=
2200
2490
2350

FIG. 31

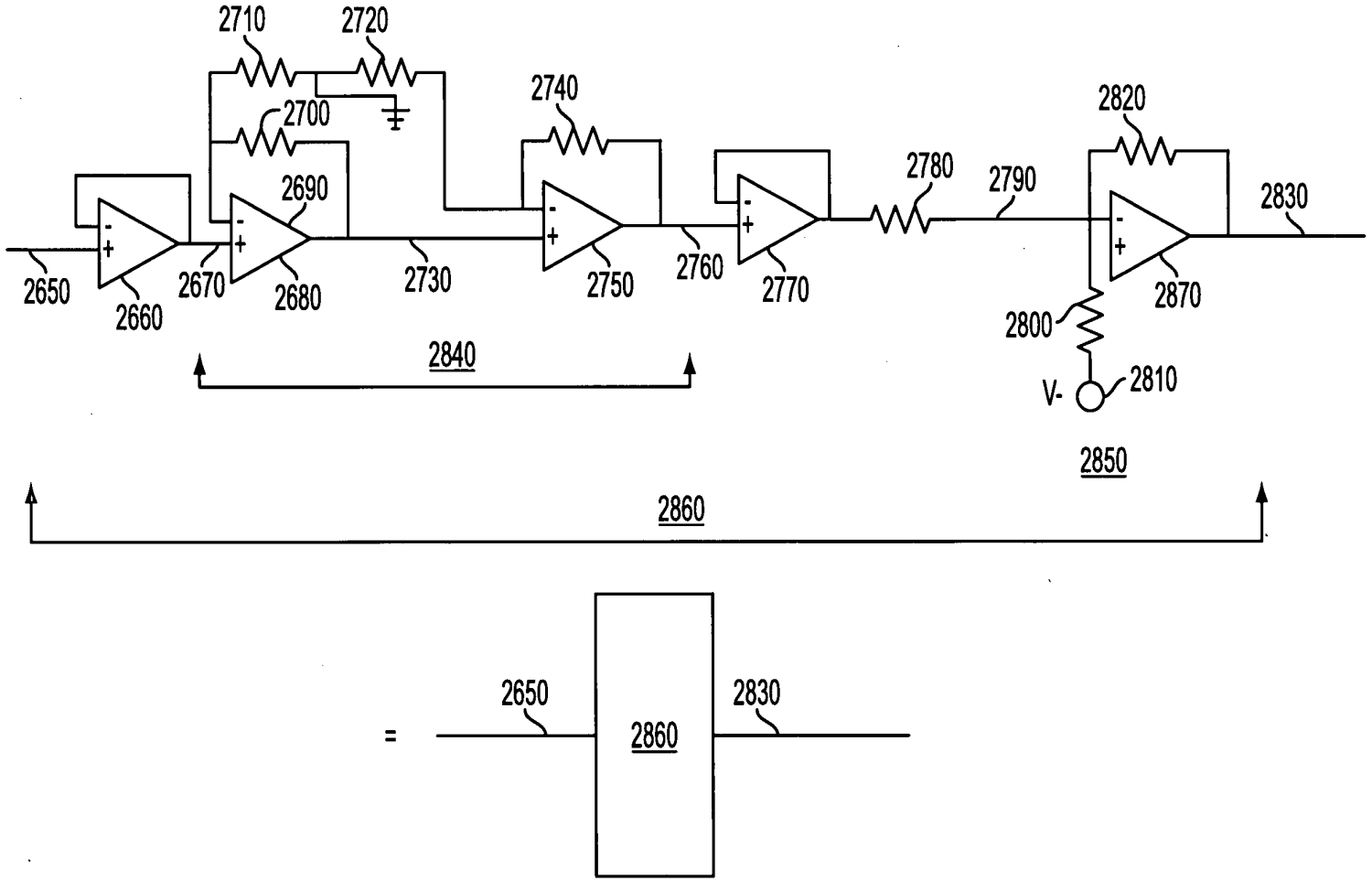
2710
2720
2700
2740
2820
2690
2780
2790
2830
2650
2660
2670
2680
2730
2750
2760
2770
2870
2800
2840
V-
2810
2850
2860
=
2650
2860
2830

FIG. 32

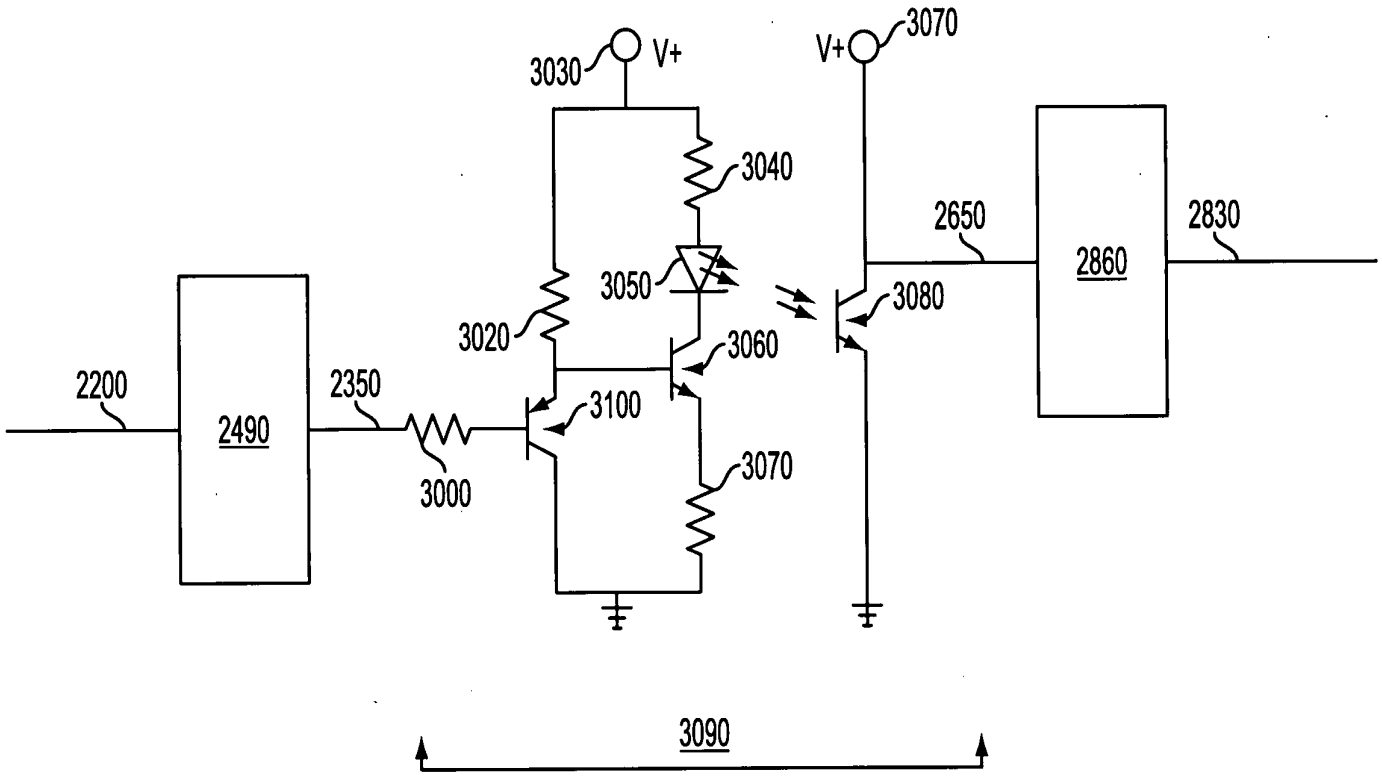
3030
V+
V+
3070
3040
2650
2860
2830
3050
3080
3020
3060
2200
2350
3100
2490
3070
3000
3090

FIG. 33

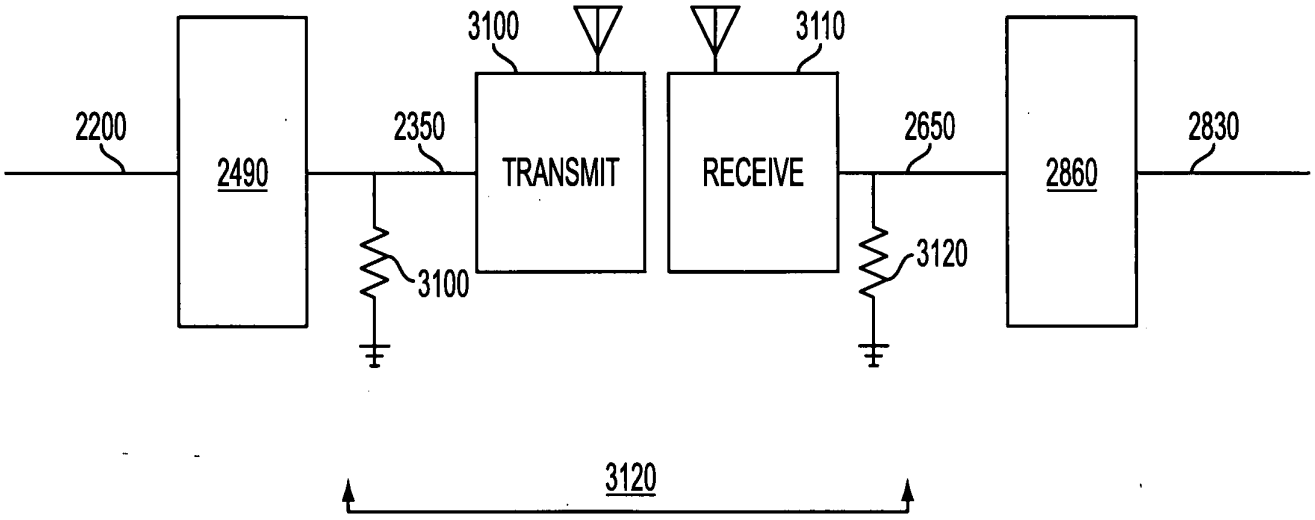
3100
3110
2200
2490
2350
TRANSMIT
RECEIVE
2650
2860
2830
3100
3120
3120

FIG. 34

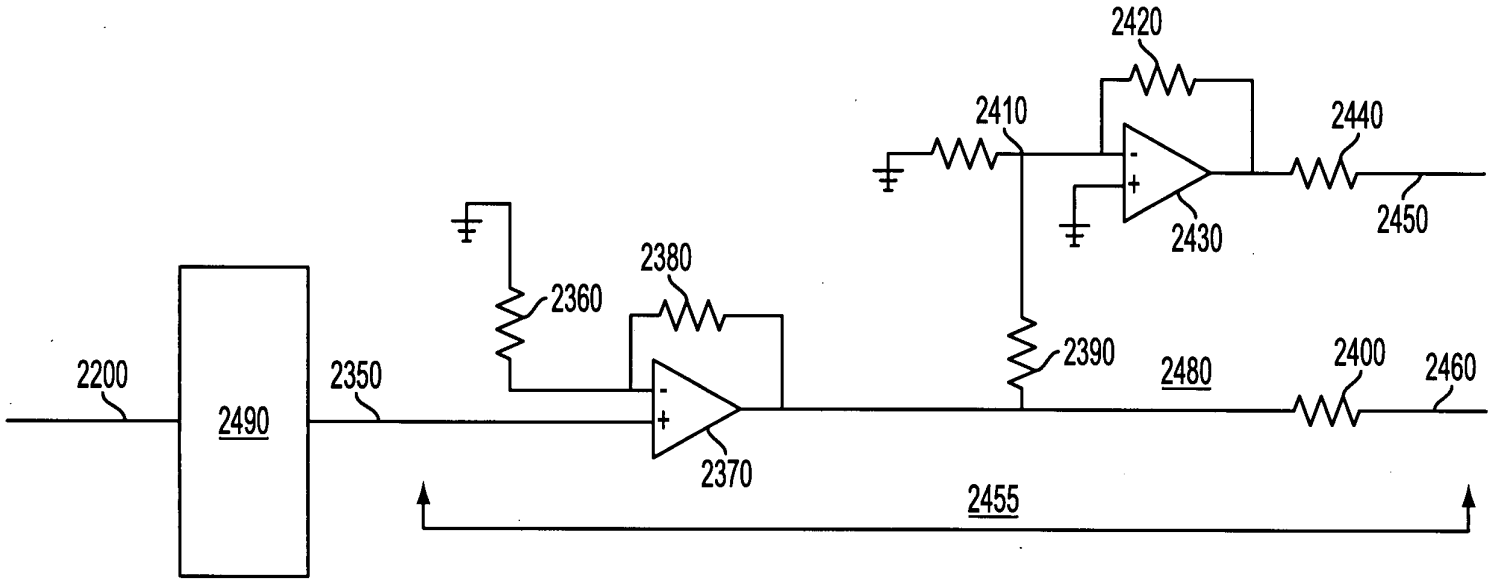
2420
2410
2440
2430
2450
2380
2360
2390
2480
2400
2460
2200
2490
2350
2370
2455

FIG. 35

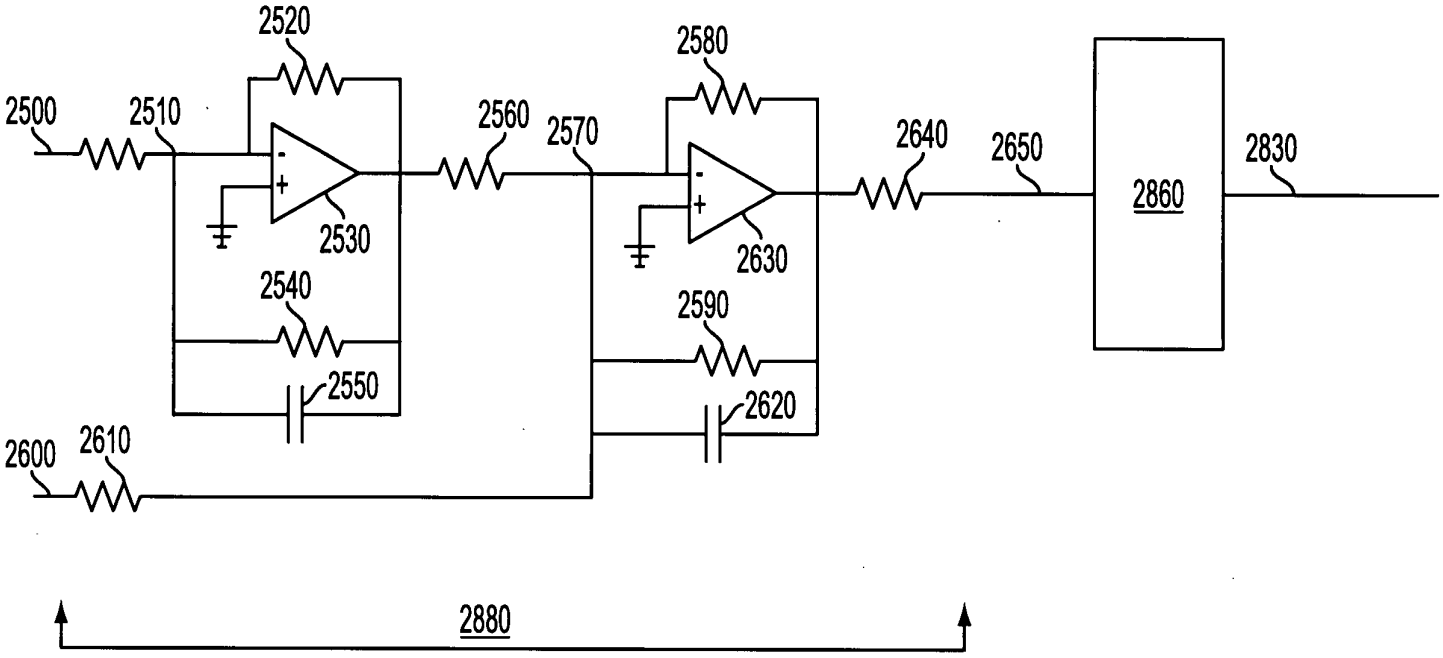
2520
2580
2500
2510
2560
2570
2640
2650
2830
2860
2530
2630
2540
2590
2550
2620
2600
2610
2880

FIG. 36

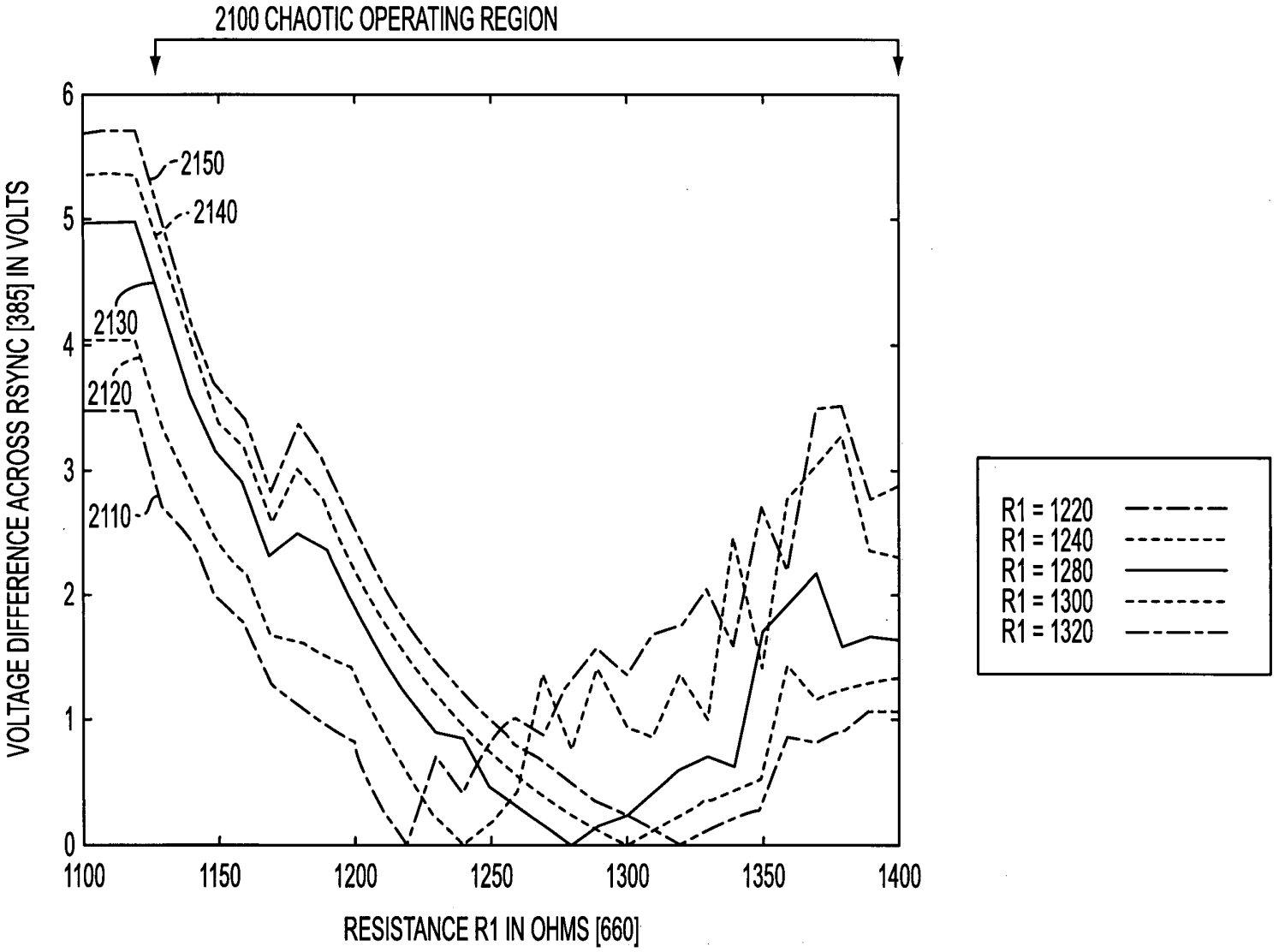
2100 CHAOTIC OPERATING REGION
VOLTAGE DIFFERENCE ACROSS RSYNC [385] IN VOLTS
RESISTANCE R1 IN OHMS [660]
2150
2140
2130
2120
2110
0
1
2
3
4
5
6
1100
1150
1200
1250
1300
1350
1400
R1 = 1220
R1 = 1240
R1 = 1280
R1 = 1300
R1 = 1320

FIG. 37A

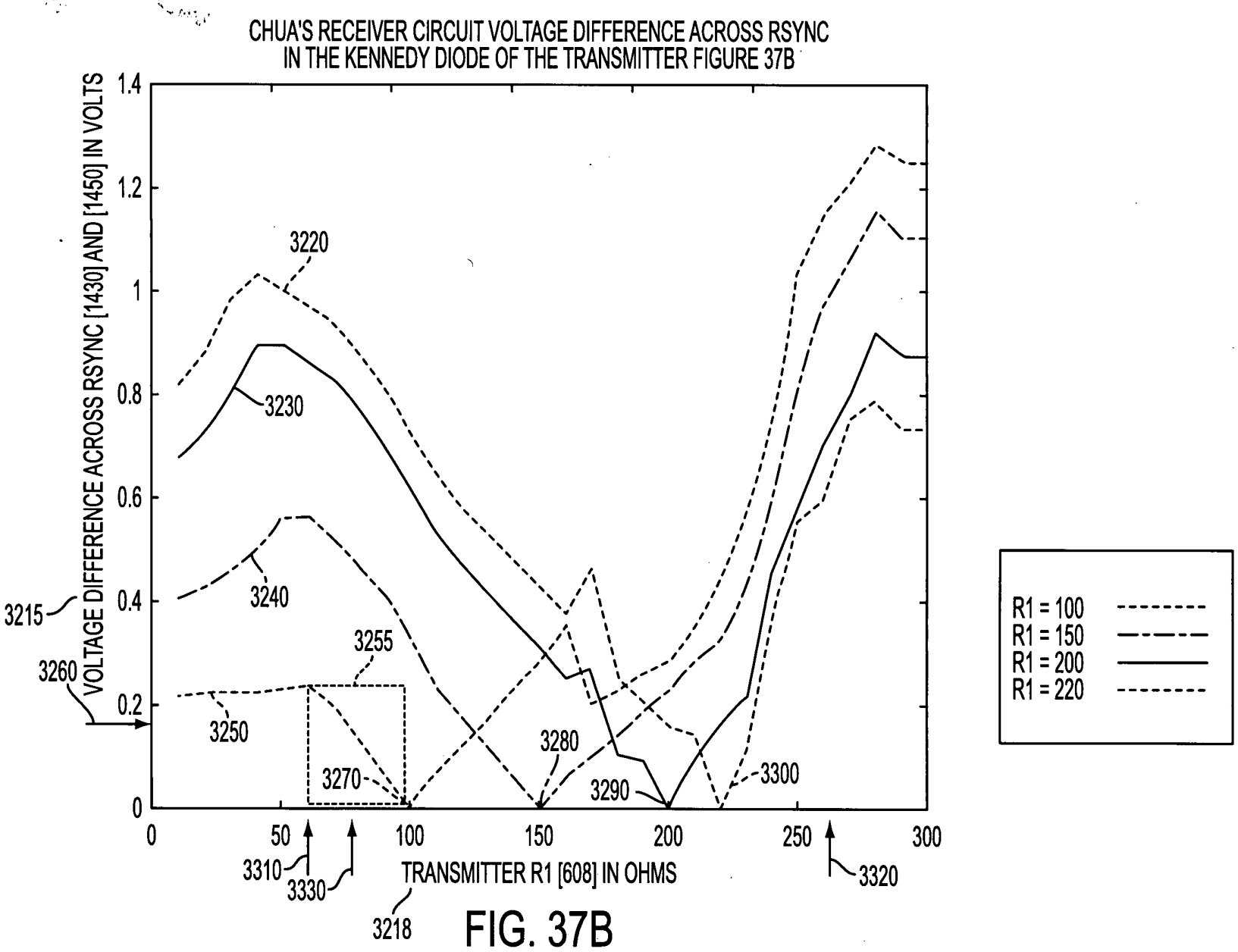
CHUA'S RECEIVER CIRCUIT VOLTAGE DIFFERENCE ACROSS RSYNC
IN THE KENNEDY DIODE OF THE TRANSMITTER FIGURE 37B
VOLTAGE DIFFERENCE ACROSS RSYNC [1430] AND [1450] IN VOLTS
TRANSMITTER R1 [608] IN OHMS
0
0.2
0.4
0.6
0.8
1
1.2
1.4
0
50
100
150
200
250
300
3215
3218
3220
3230
3240
3250
3255
3260
3270
3280
3290
3300
3310
3320
3330
R1 = 100
R1 = 150
R1 = 200
R1 = 220

FIG. 37B

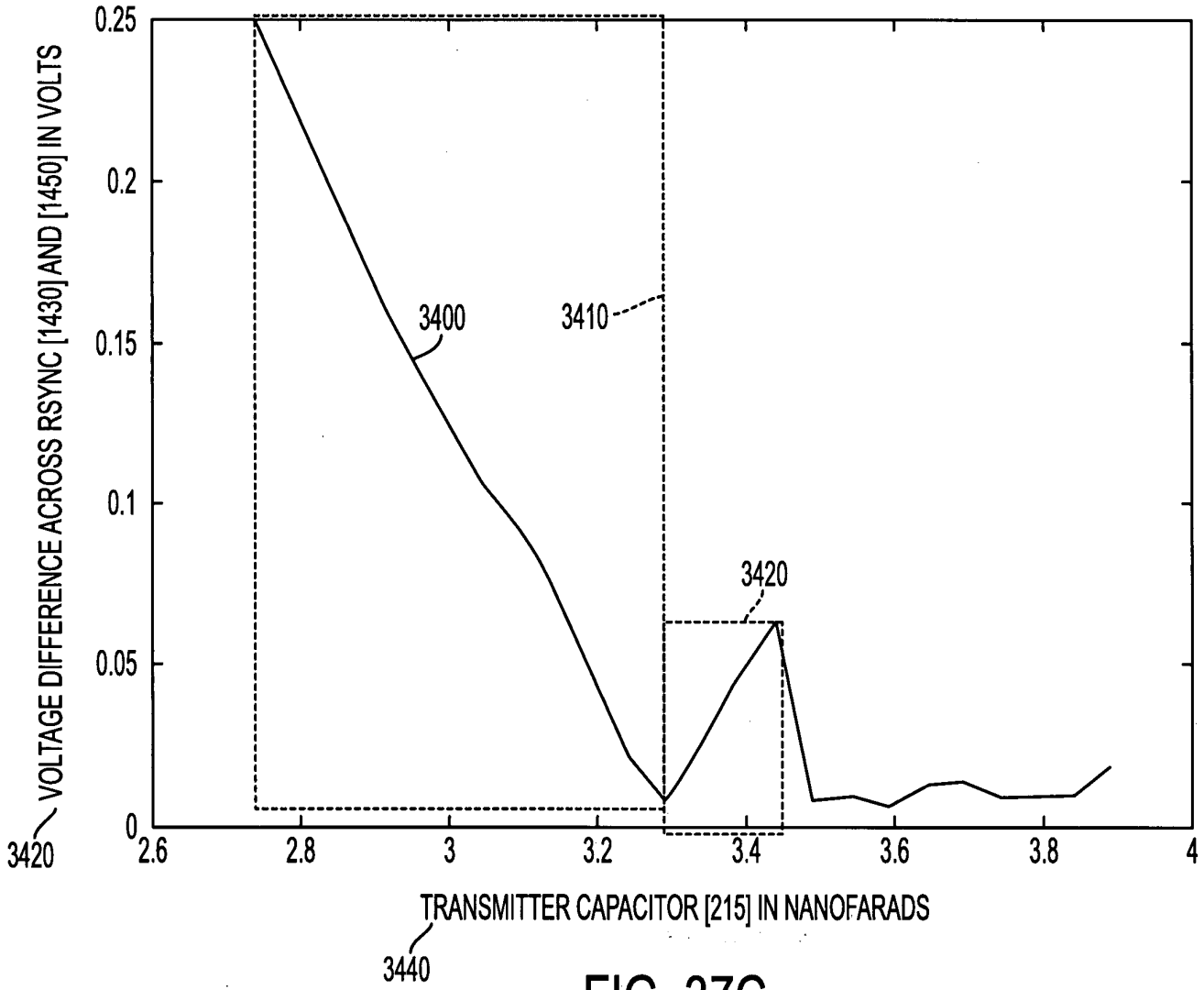
0.25
0.2
0.15
0.1
0.05
0
2.6
2.8
3
3.2
3.4
3.6
3.8
4
VOLTAGE DIFFERENCE ACROSS RSYNC [1430] AND [1450] IN VOLTS
TRANSMITTER CAPACITOR [215] IN NANOFARADS
3400
3410
3420
3420
3440

FIG. 37C

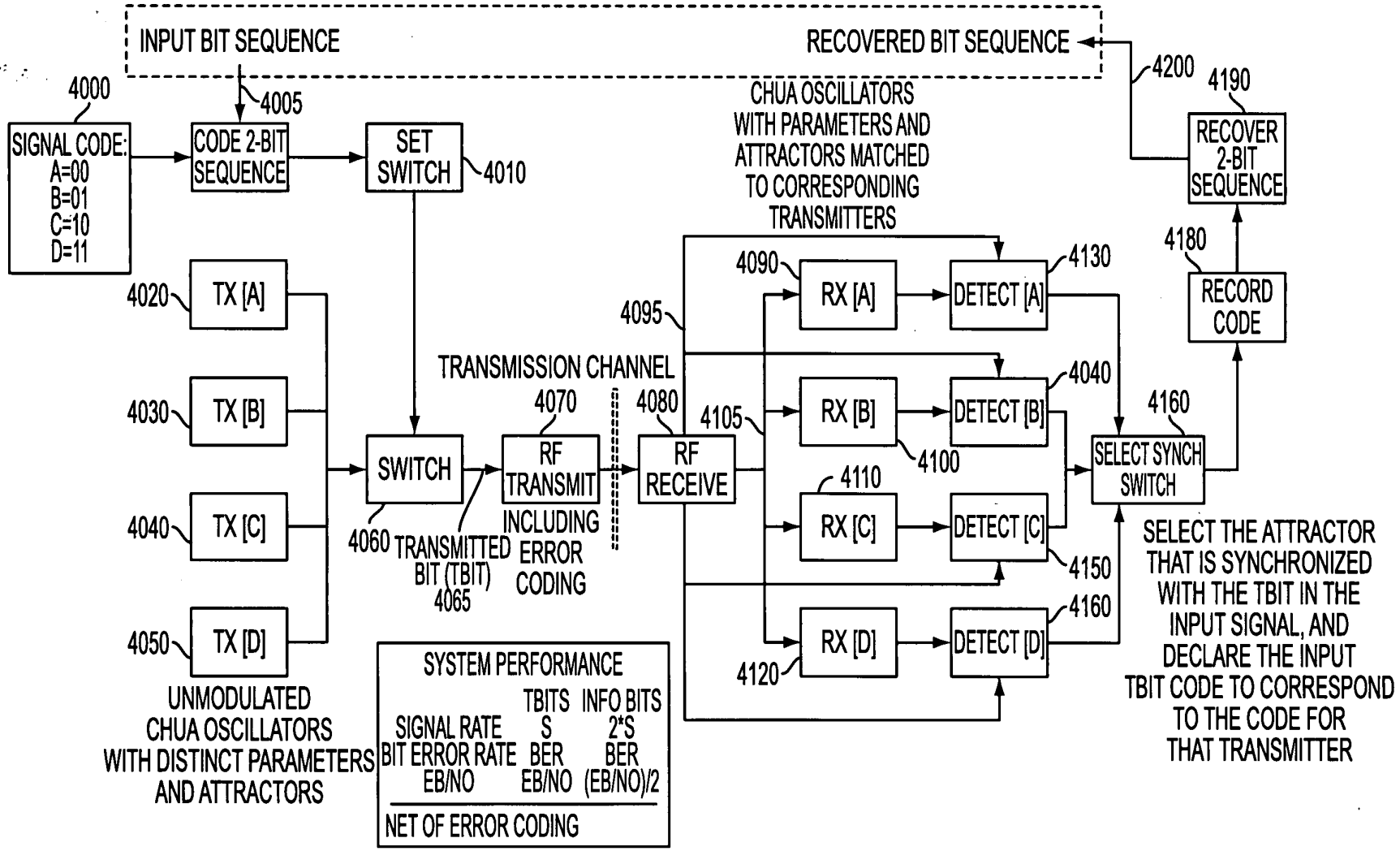
INPUT BIT SEQUENCE
RECOVERED BIT SEQUENCE
4000
SIGNAL CODE:
A=00
B=01
C=10
D=11
4005
CODE 2-BIT SEQUENCE
SET SWITCH
4010
CHUA OSCILLATORS WITH PARAMETERS AND ATTRACTORS MATCHED TO CORRESPONDING TRANSMITTERS
4200
4190
RECOVER 2-BIT SEQUENCE
4180
RECORD CODE
4020
TX [A]
4030
TX [B]
4040
TX [C]
4050
TX [D]
SWITCH
4060
TRANSMITTED BIT (TBIT) 4065
4070
RF TRANSMIT
INCLUDING ERROR CODING
TRANSMISSION CHANNEL
4080
RF RECEIVE
4095
4090
RX [A]
DETECT [A]
4130
4105
RX [B]
DETECT [B]
4040
4100
4110
RX [C]
DETECT [C]
4150
4120
RX [D]
DETECT [D]
4160
4160
SELECT SYNCH SWITCH
SELECT THE ATTRACTOR THAT IS SYNCHRONIZED WITH THE TBIT IN THE INPUT SIGNAL, AND DECLARE THE INPUT TBIT CODE TO CORRESPOND TO THE CODE FOR THAT TRANSMITTER
UNMODULATED CHUA OSCILLATORS WITH DISTINCT PARAMETERS AND ATTRACTORS
SYSTEM PERFORMANCE
TBITS
INFO BITS
SIGNAL RATE
S
2*S
BIT ERROR RATE
BER
BER
EB/NO
EB/NO
(EB/NO)/2
NET OF ERROR CODING

FIG. 38

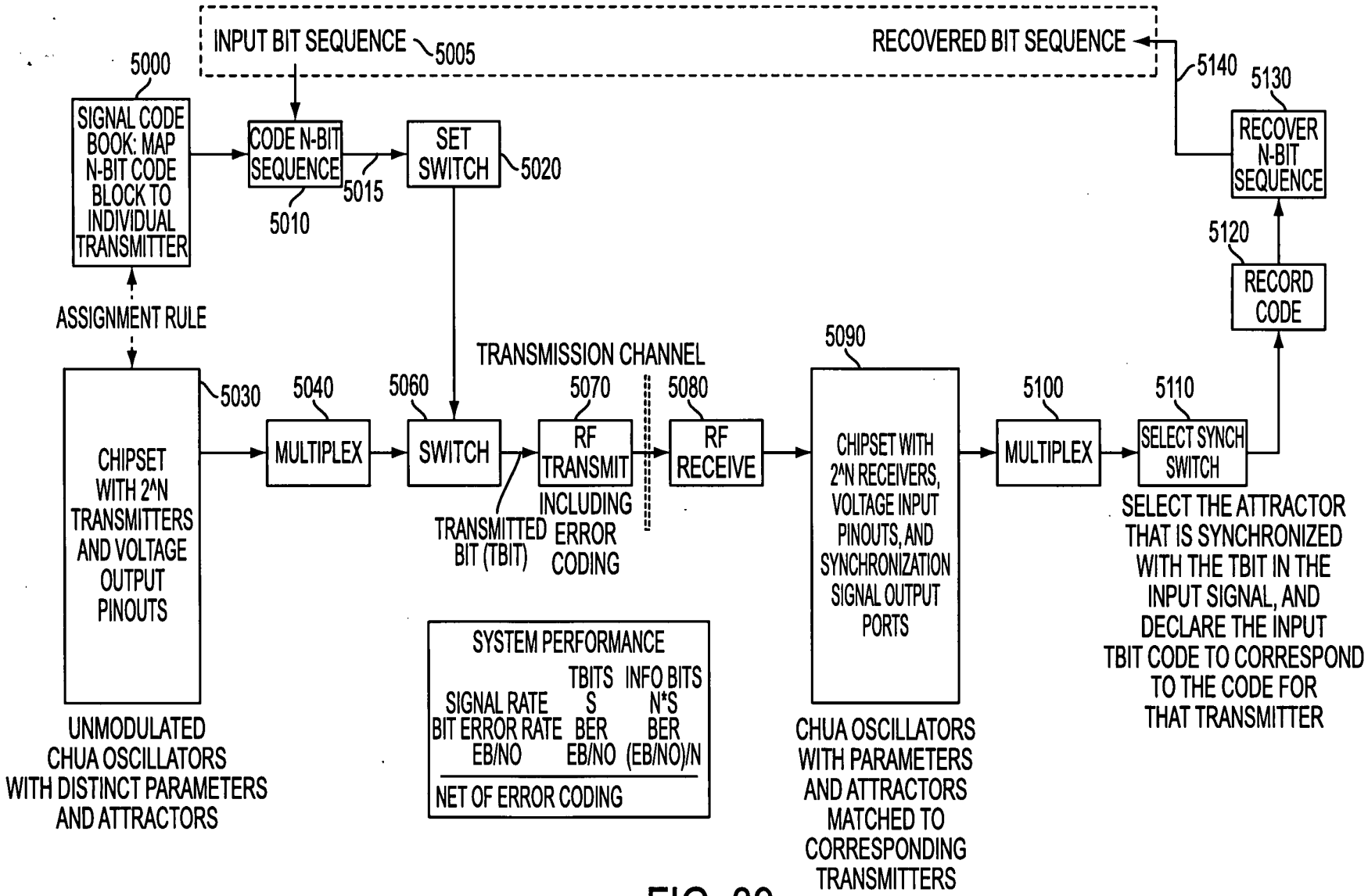
INPUT BIT SEQUENCE
5005
RECOVERED BIT SEQUENCE
5140
5000
SIGNAL CODE BOOK: MAP N-BIT CODE BLOCK TO INDIVIDUAL TRANSMITTER
CODE N-BIT SEQUENCE
5010
5015
SET SWITCH
5020
5130
RECOVER N-BIT SEQUENCE
5120
RECORD CODE
ASSIGNMENT RULE
TRANSMISSION CHANNEL
5090
5030
5040
5060
5070
5080
5100
5110
CHIPSET WITH 2^N TRANSMITTERS AND VOLTAGE OUTPUT PINOUTS
MULTIPLEX
SWITCH
RF TRANSMIT
RF RECEIVE
CHIPSET WITH 2^N RECEIVERS, VOLTAGE INPUT PINOUTS, AND SYNCHRONIZATION SIGNAL OUTPUT PORTS
MULTIPLEX
SELECT SYNCH SWITCH
TRANSMITTED BIT (TBIT)
INCLUDING ERROR CODING
SELECT THE ATTRACTOR THAT IS SYNCHRONIZED WITH THE TBIT IN THE INPUT SIGNAL, AND DECLARE THE INPUT TBIT CODE TO CORRESPOND TO THE CODE FOR THAT TRANSMITTER
SYSTEM PERFORMANCE
SIGNAL RATE
BIT ERROR RATE
EB/NO
TBITS S
BER
EB/NO
INFO BITS N*S
BER
(EB/NO)/N
NET OF ERROR CODING
UNMODULATED CHUA OSCILLATORS WITH DISTINCT PARAMETERS AND ATTRACTORS
CHUA OSCILLATORS WITH PARAMETERS AND ATTRACTORS MATCHED TO CORRESPONDING TRANSMITTERS

FIG. 39

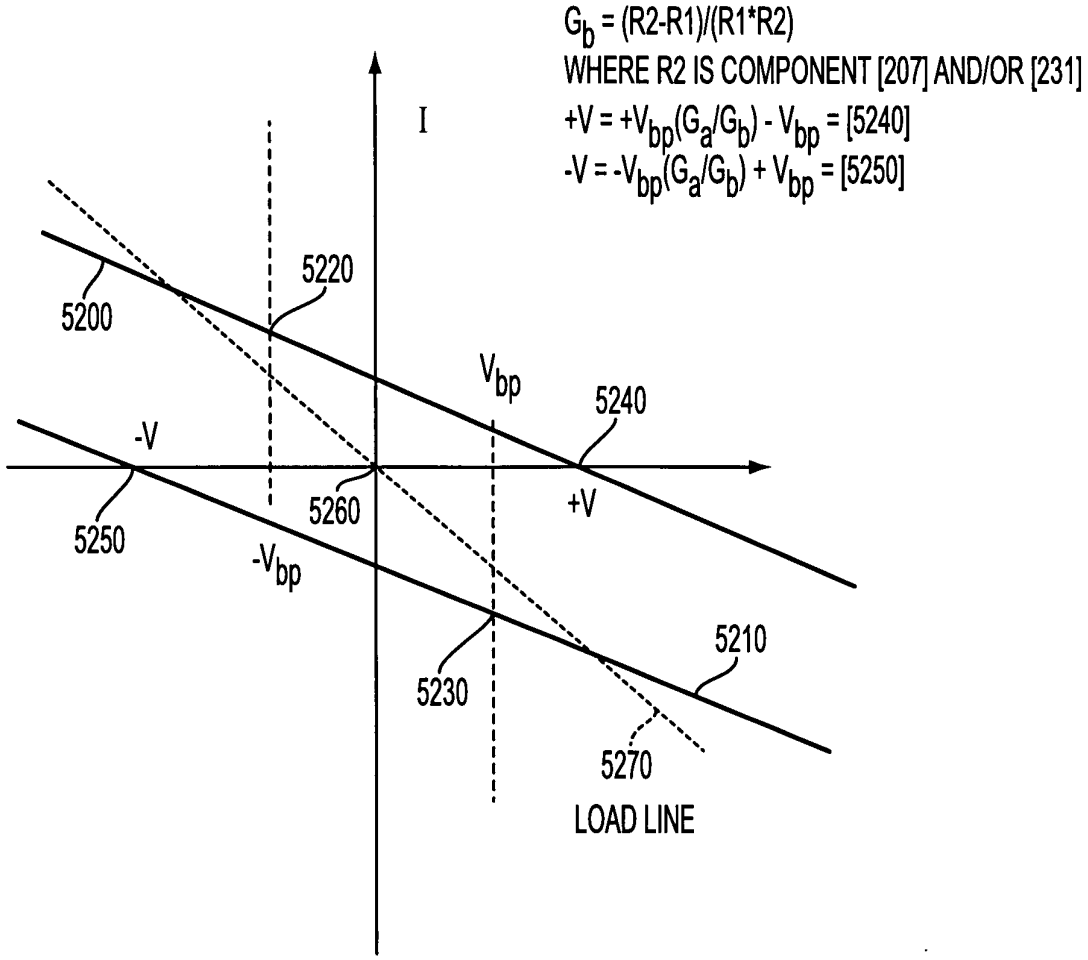
$G_b = (R2-R1)/(R1*R2)$
WHERE R2 IS COMPONENT [207] AND/OR [231]
$+V = +V_{bp}(G_a/G_b) - V_{bp}$ = [5240]
$-V = -V_{bp}(G_a/G_b) + V_{bp}$ = [5250]
I
5200
5220
V_{bp}
5240
-V
5250
5260
+V
$-V_{bp}$
5210
5230
5270
LOAD LINE

FIG. 40

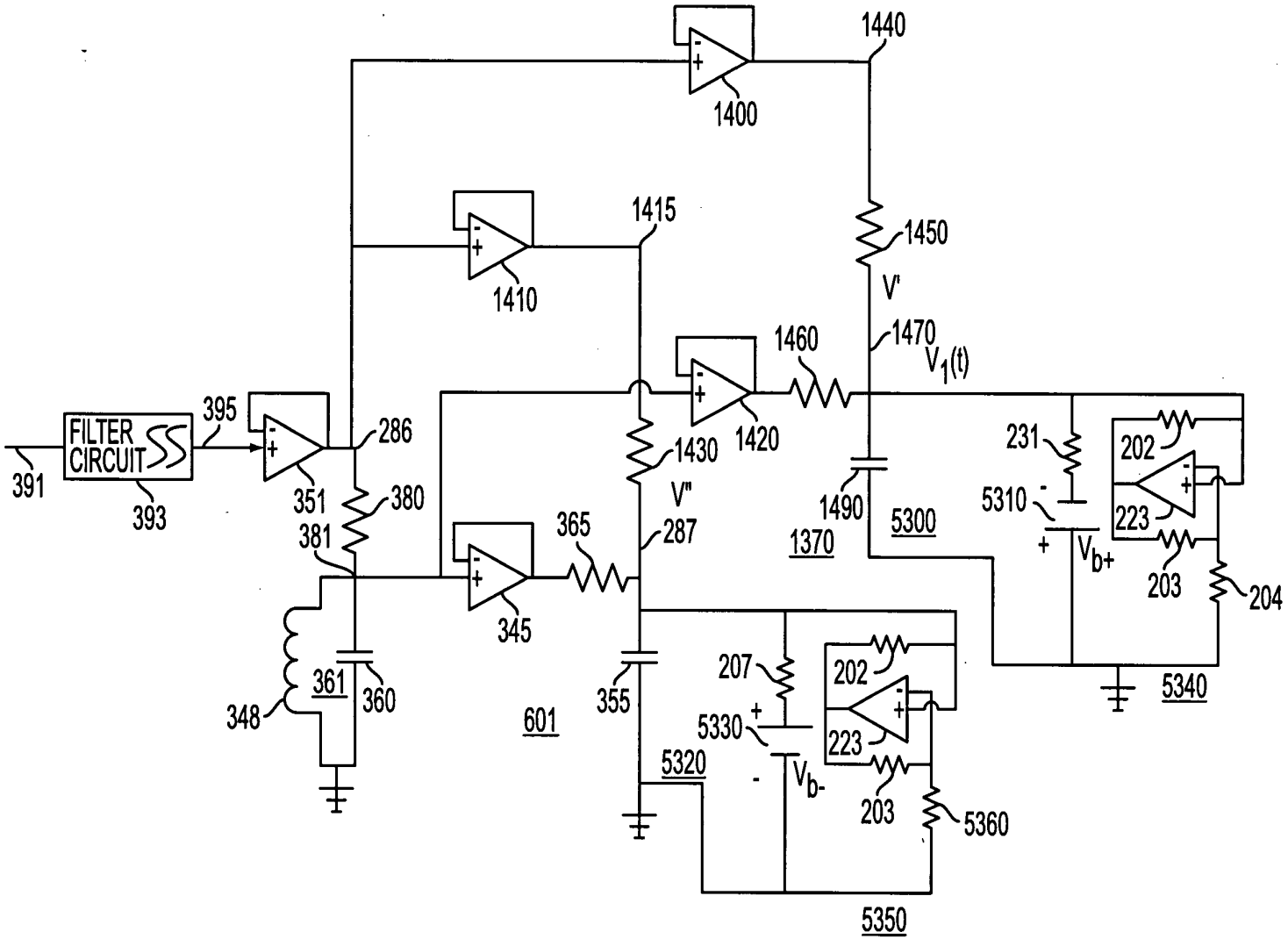
1440
1400
1415
1410
1450
V'
1460
1470
$V_1(t)$
1420
1430
V"
FILTER CIRCUIT
391
393
395
351
286
380
381
365
287
345
1490
1370
5300
231
5310
202
223
203
204
V_{b+}
5340
361
348
360
601
355
207
5330
5320
V_{b-}
5360
5350

FIG. 41

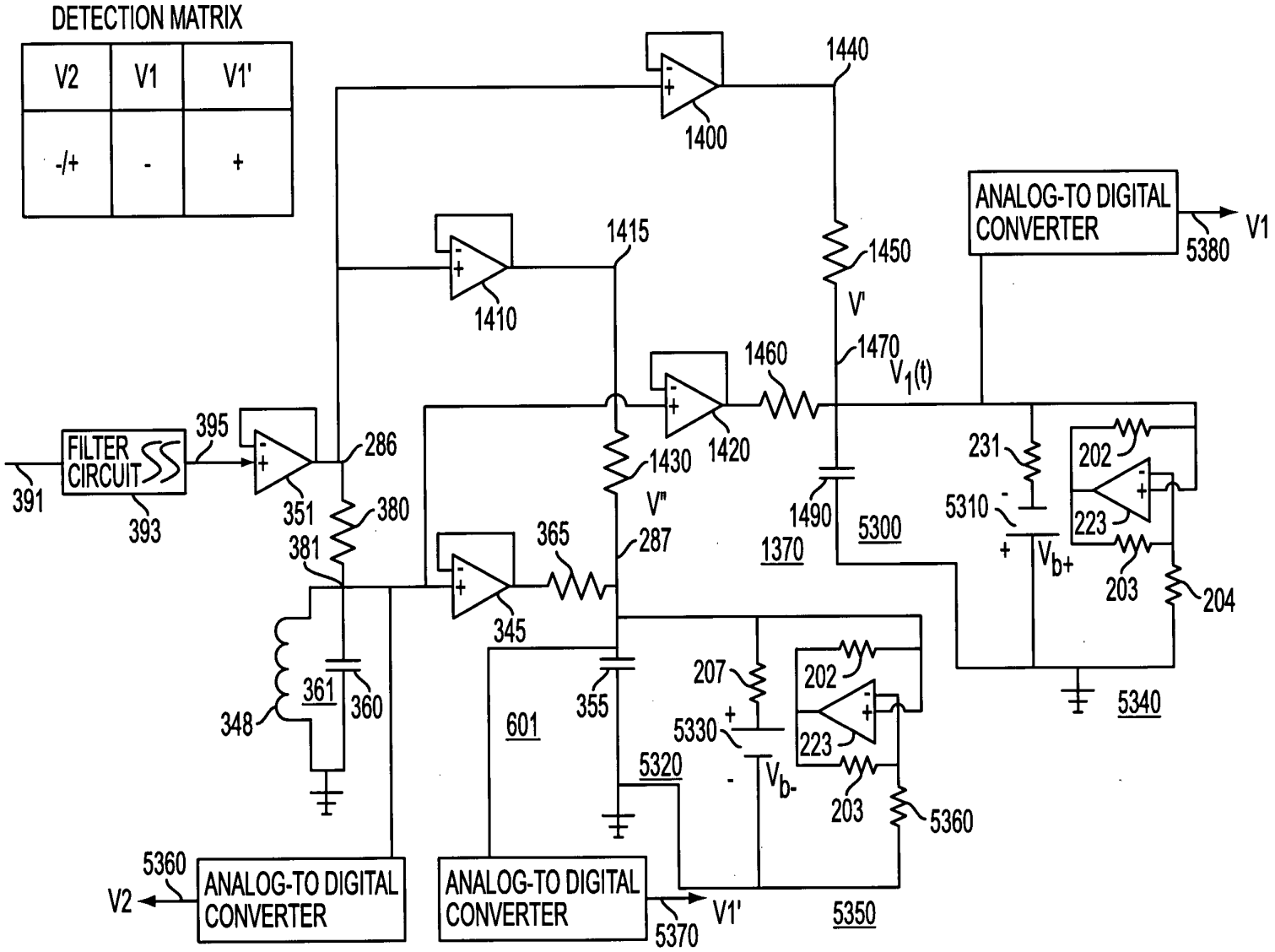
DETECTION MATRIX
V2
V1
V1'
-/+
-
+
1440
1400
1415
1410
1450
V'
1470
$V_1(t)$
1460
1420
1430
V"
1490
1370
5300
ANALOG-TO DIGITAL CONVERTER
5380
V1
231
5310
V_{b+}
202
223
203
204
5340
FILTER CIRCUIT
391
393
395
351
286
380
381
365
287
345
361
360
348
355
601
207
5330
V_{b-}
5320
5360
5350
ANALOG-TO DIGITAL CONVERTER
5360
V2
ANALOG-TO DIGITAL CONVERTER
5370
V1'

FIG. 42

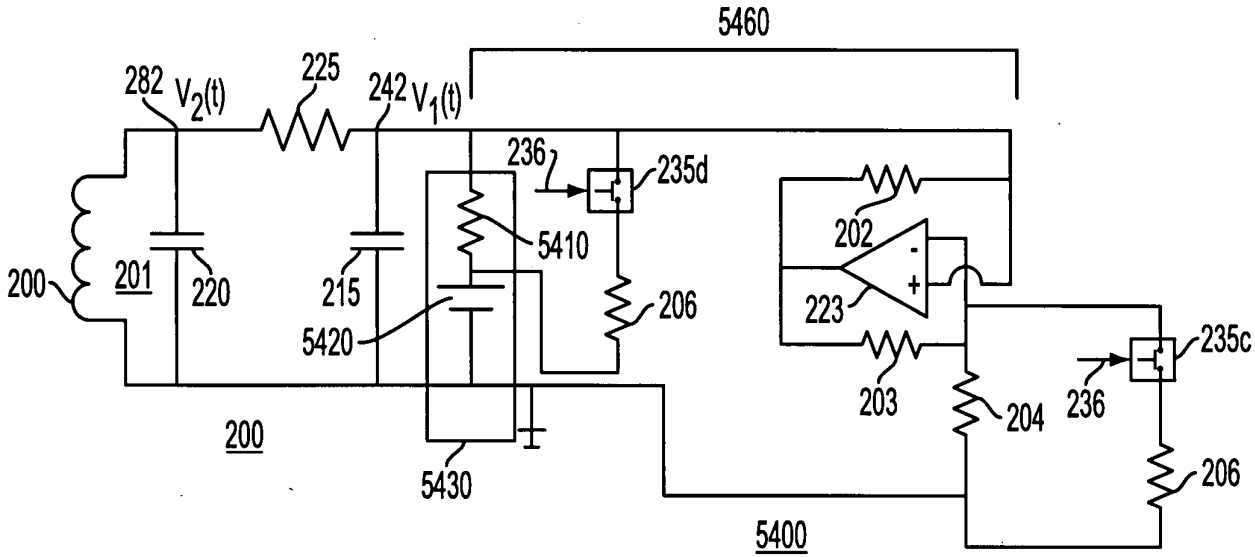
5460
282
$V_2(t)$
225
242
$V_1(t)$
236
235d
5410
206
200
201
220
215
5420
202
223
203
204
236
235c
206
200
5430
5400

FIG. 43

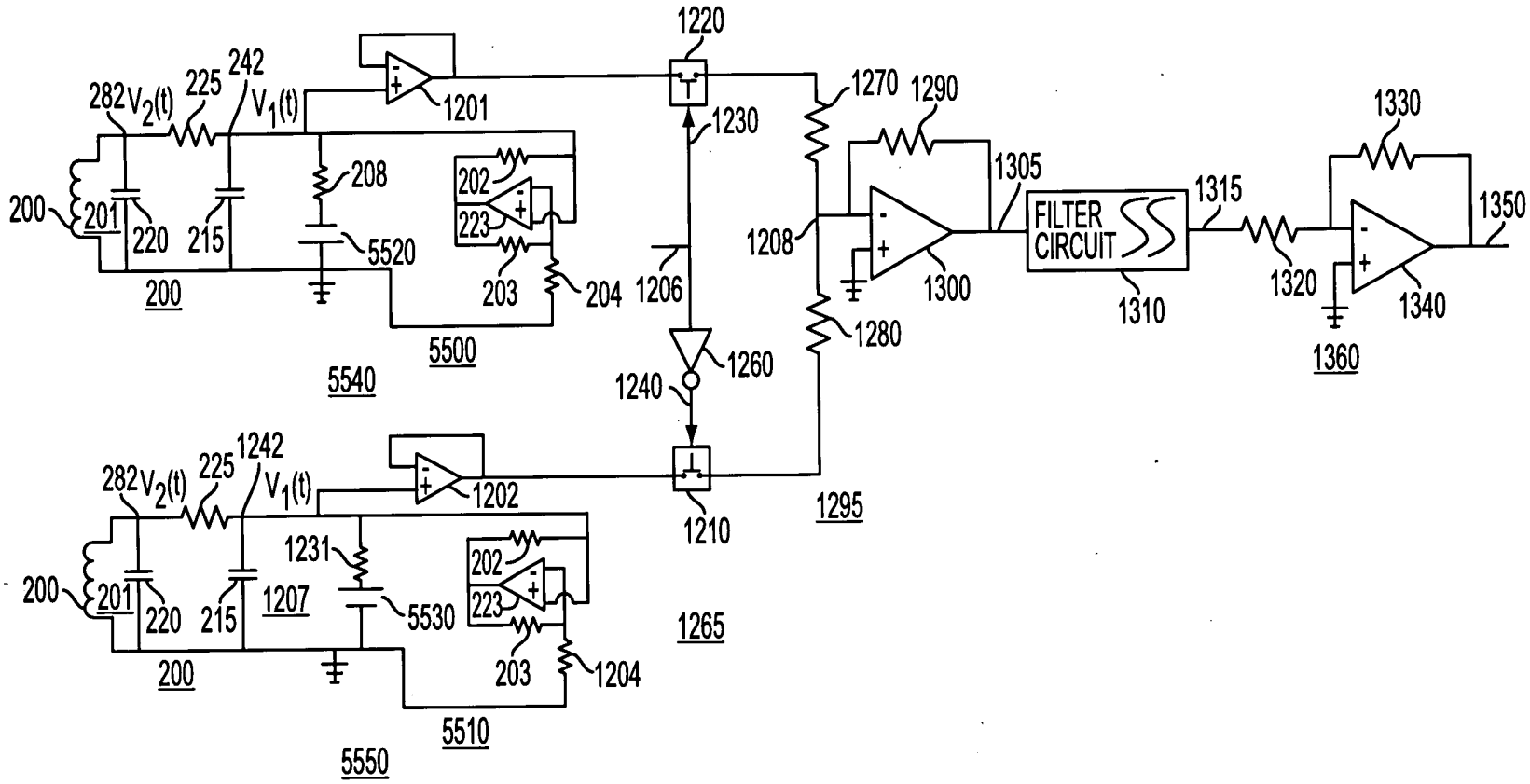
1220
282 $V_2(t)$
225
242
$V_1(t)$
1201
1230
1270
1290
1330
1305
1315
1350
200
201
220
215
208
202
223
5520
1208
FILTER CIRCUIT
200
203
204
1206
1300
1320
1340
5500
1280
1310
1360
5540
1240
1260
1242
282 $V_2(t)$
225
$V_1(t)$
1202
1295
1210
1231
1207
5530
1265
200
201
220
215
1204
203
5510
5550

FIG. 44

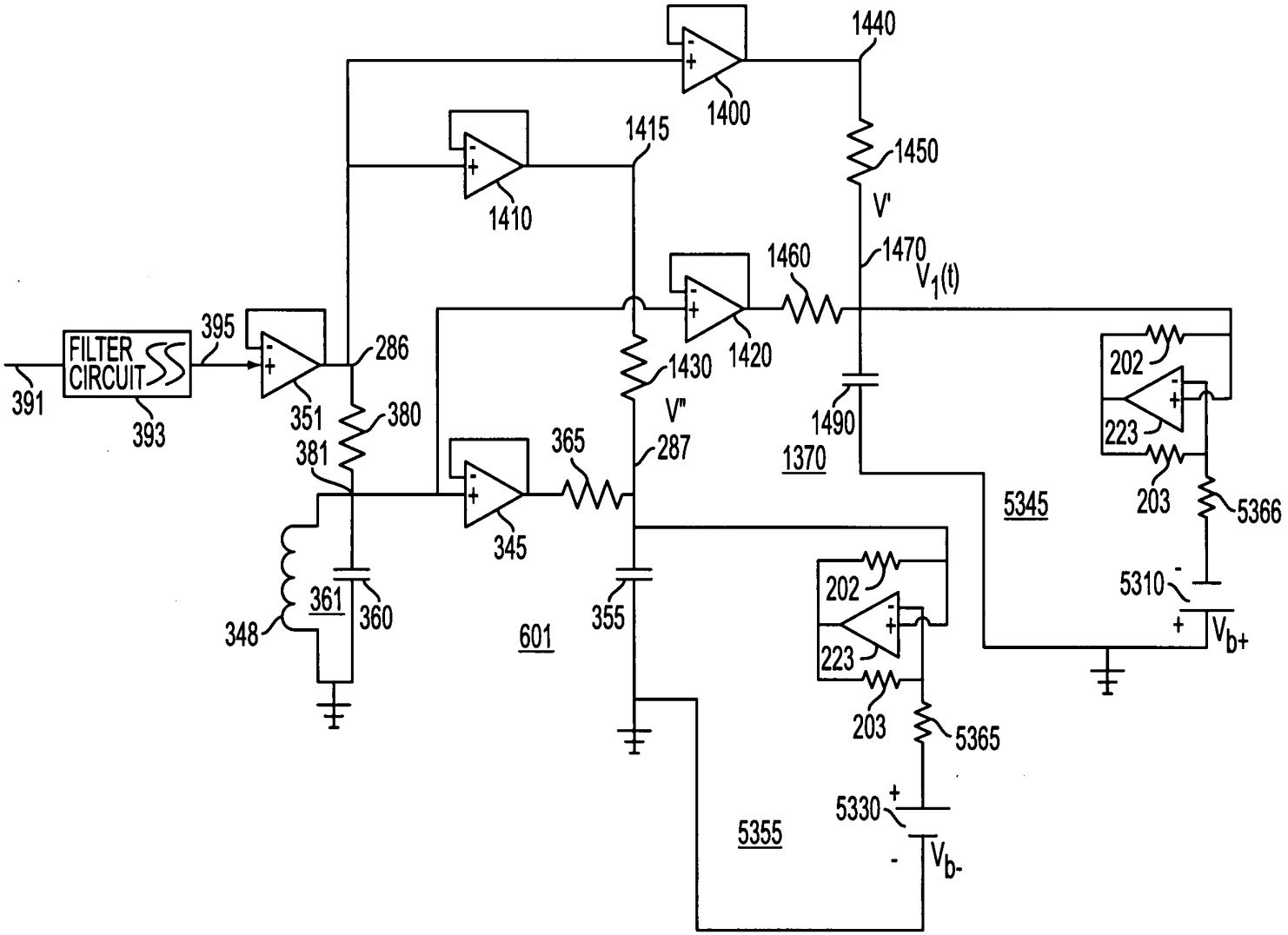
1440
1400
1415
1450
1410
V'
1460
1470
$V_1(t)$
1420
1430
V"
FILTER CIRCUIT
395
286
391
393
351
380
381
365
287
1490
1370
345
202
223
203
5366
5345
361
348
360
355
601
5310
V_{b+}
202
223
203
5365
5330
5355
V_{b-}

FIG. 45A

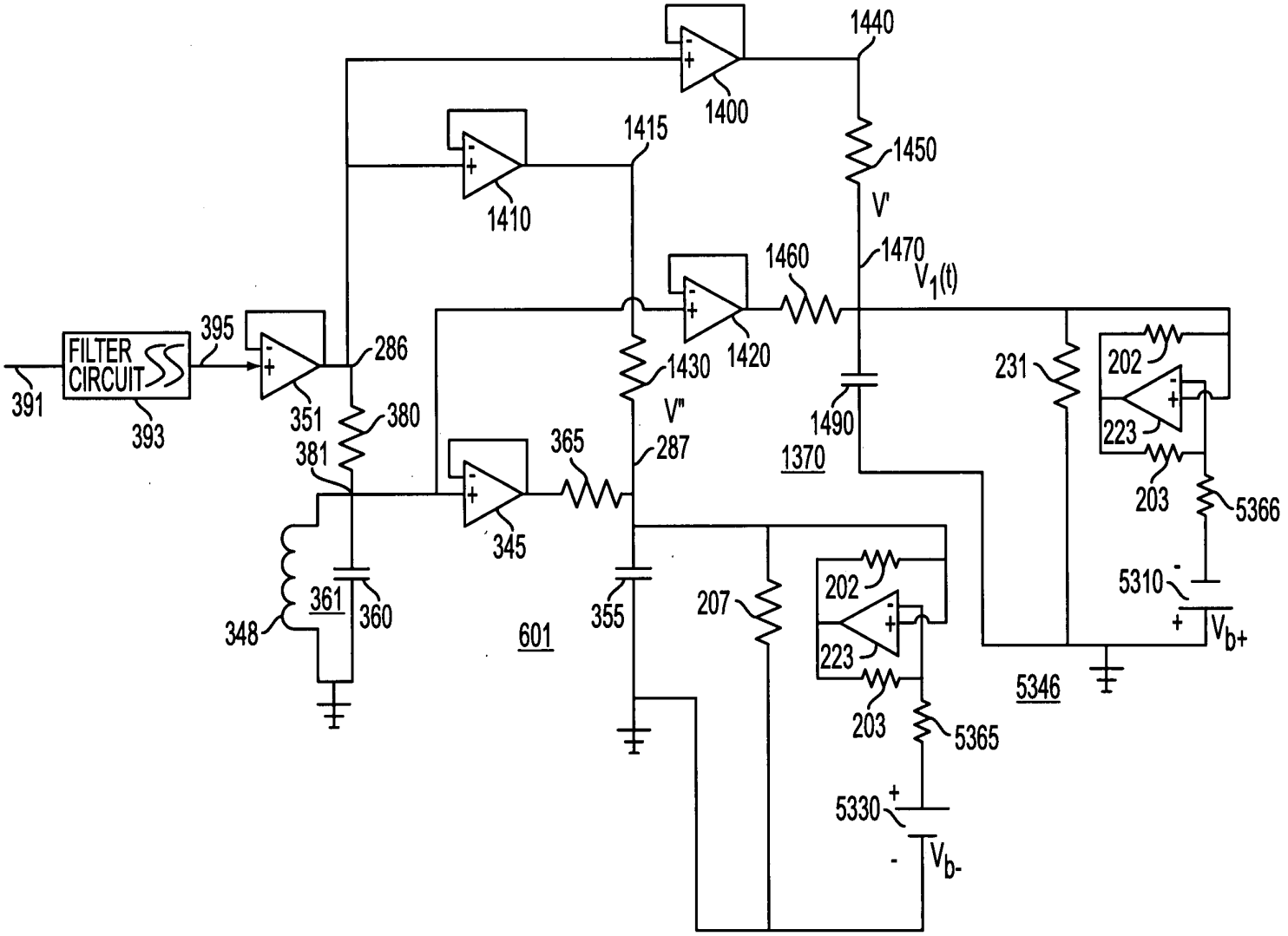
1440
1400
1415
1450
1410
V'
1460
1470
$V_1(t)$
1420
1430
V"
1490
1370
231
202
223
203
5366
5310
V_{b+}
5346
FILTER CIRCUIT
391
393
395
351
286
380
381
365
345
287
348
361
360
355
601
207
202
223
203
5365
5330
V_{b-}
5356

FIG. 45B

$G_b = (R2-R1)/(R1*R2) = G_a-(1/R2)$
WHERE R2 IS COMPONENT [207] AND/OR [231]
$+V = +V_{bp}(G_a/G_b) - V_{bp}$ = [5240]
$-V = -V_{bp}(G_a/G_b) + V_{bp}$ = [5250]

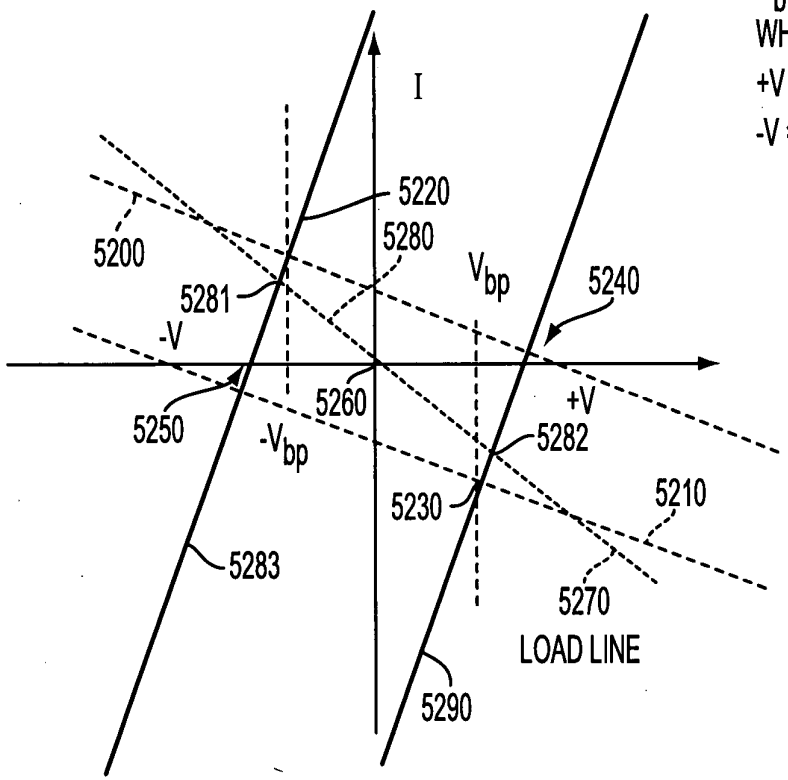

FIG. 46

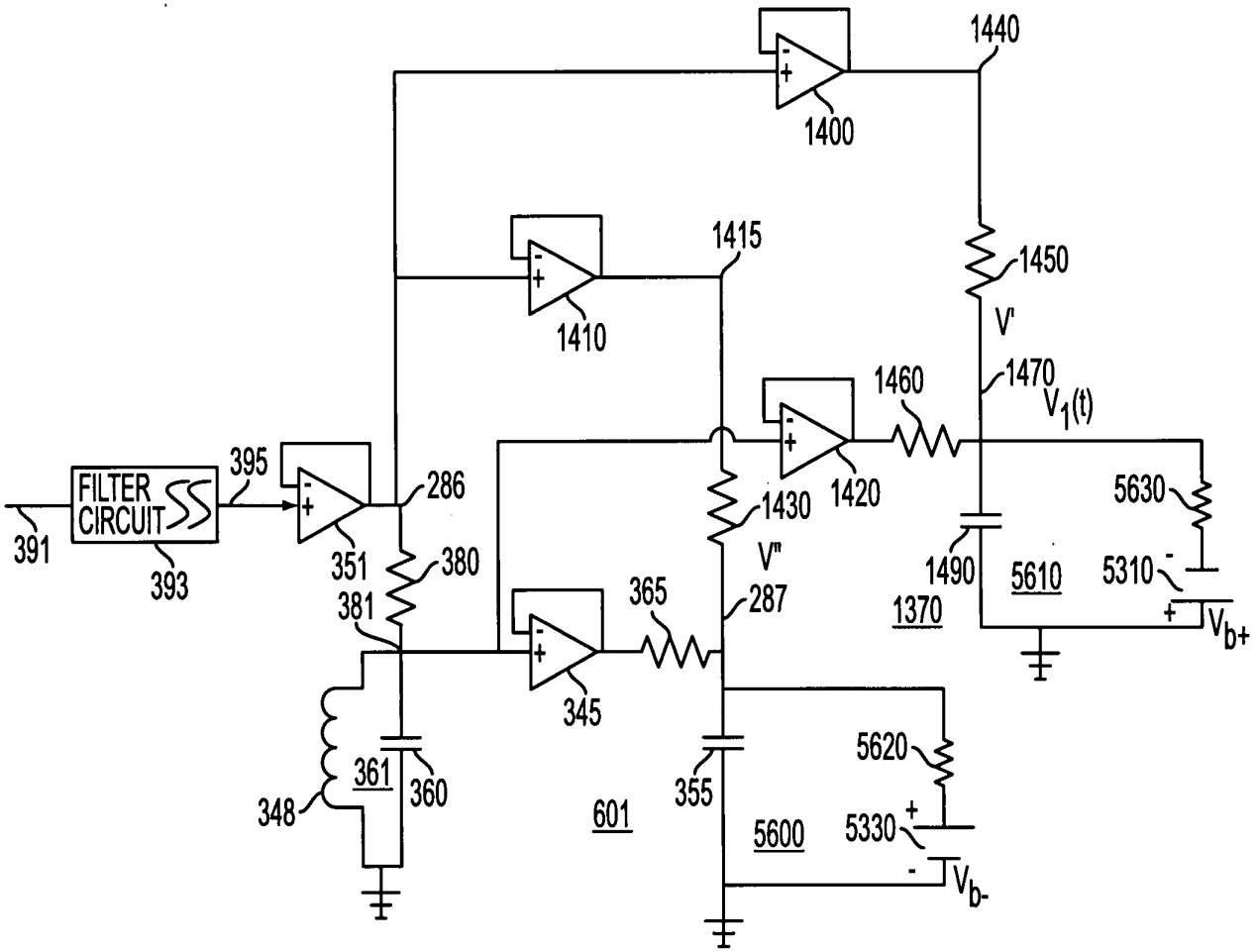
1440
1400
1415
1410
1450
V'
1460
1470
$V_1(t)$
1420
1430
V"
395
FILTER CIRCUIT
391
393
351
286
380
381
365
287
345
361
360
348
355
601
5620
5330
5600
V_{b-}
1490
5610
1370
5630
5310
V_{b+}

FIG. 47

DETECTION MATRIX

V2	V1	V1'
-/+	+	-

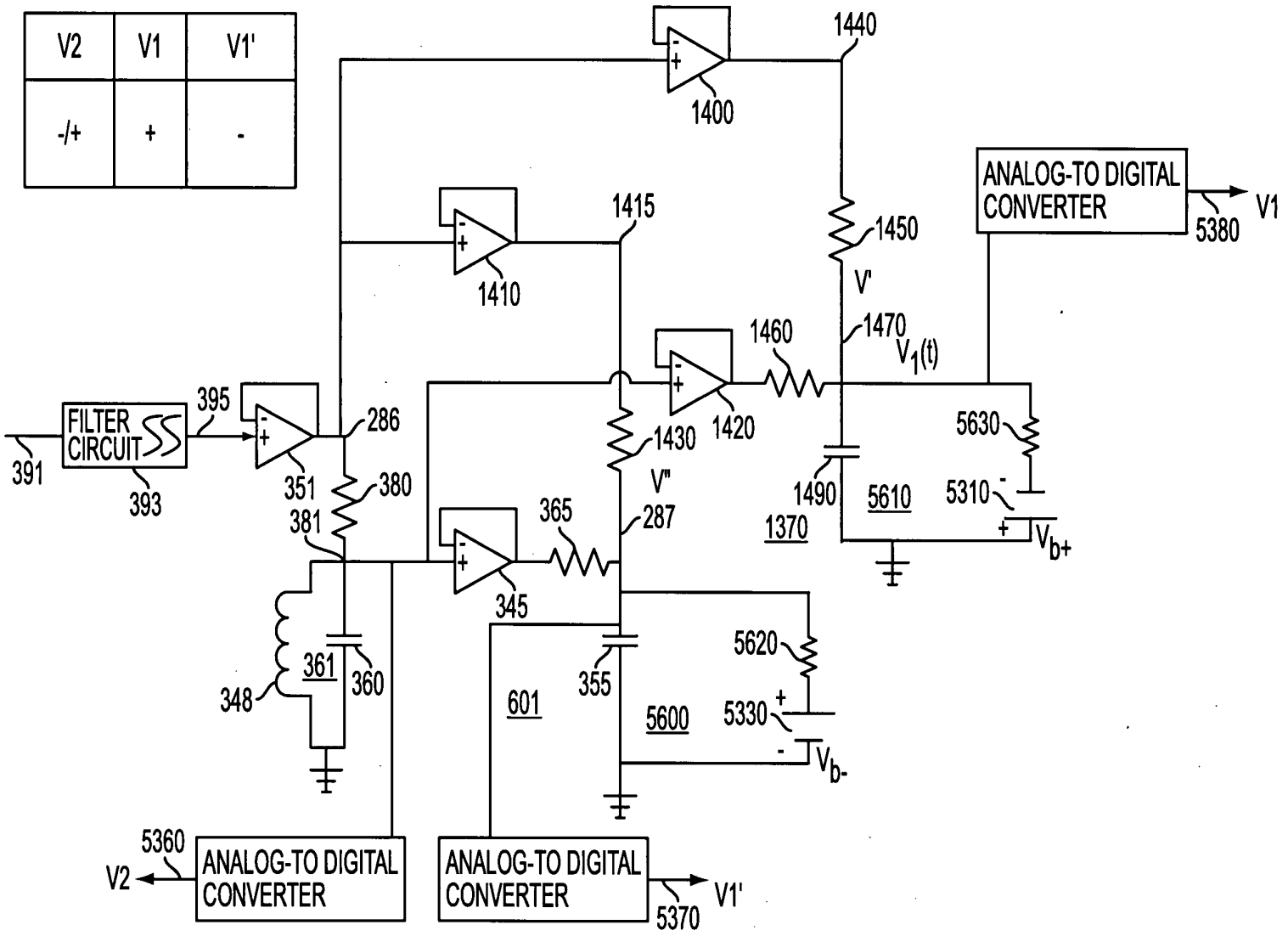

FIG. 48

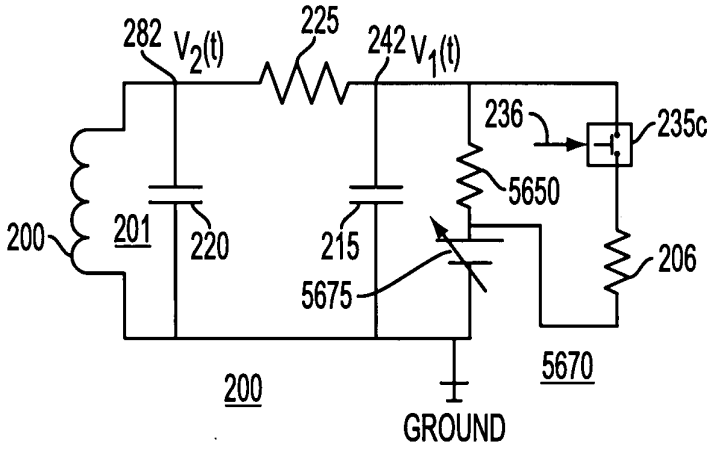
282
$V_2(t)$
225
242
$V_1(t)$
236
235c
5650
200
201
220
215
206
5675
5670
200
GROUND

FIG. 49

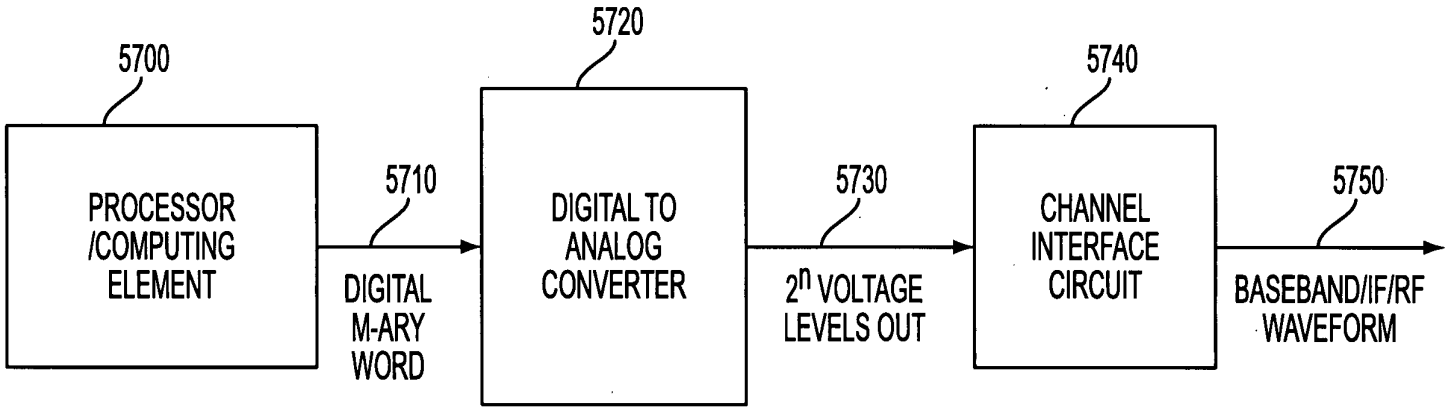
5700
PROCESSOR /COMPUTING ELEMENT
5710
DIGITAL M-ARY WORD
5720
DIGITAL TO ANALOG CONVERTER
5730
2^n VOLTAGE LEVELS OUT
5740
CHANNEL INTERFACE CIRCUIT
5750
BASEBAND/IF/RF WAVEFORM

FIG. 50

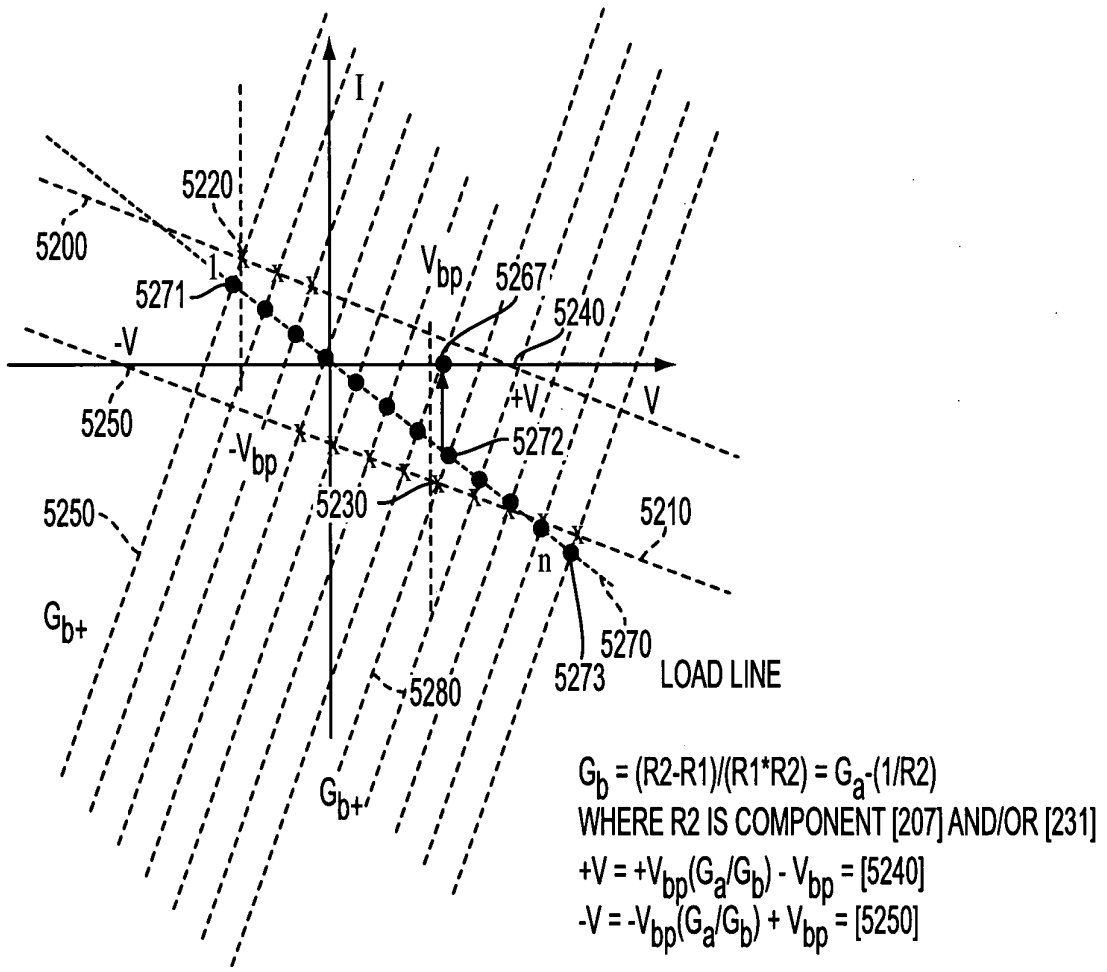
I
5220
5200
1
5271
V_{bp}
5267
5240
-V
+V
V
5250
$-V_{bp}$
5272
5230
5250
5210
n
G_{b+}
5270
5273
LOAD LINE
5280
G_{b+}
$G_b = (R2-R1)/(R1*R2) = G_a-(1/R2)$
WHERE R2 IS COMPONENT [207] AND/OR [231]
$+V = +V_{bp}(G_a/G_b) - V_{bp}$ = [5240]
$-V = -V_{bp}(G_a/G_b) + V_{bp}$ = [5250]

FIG. 51

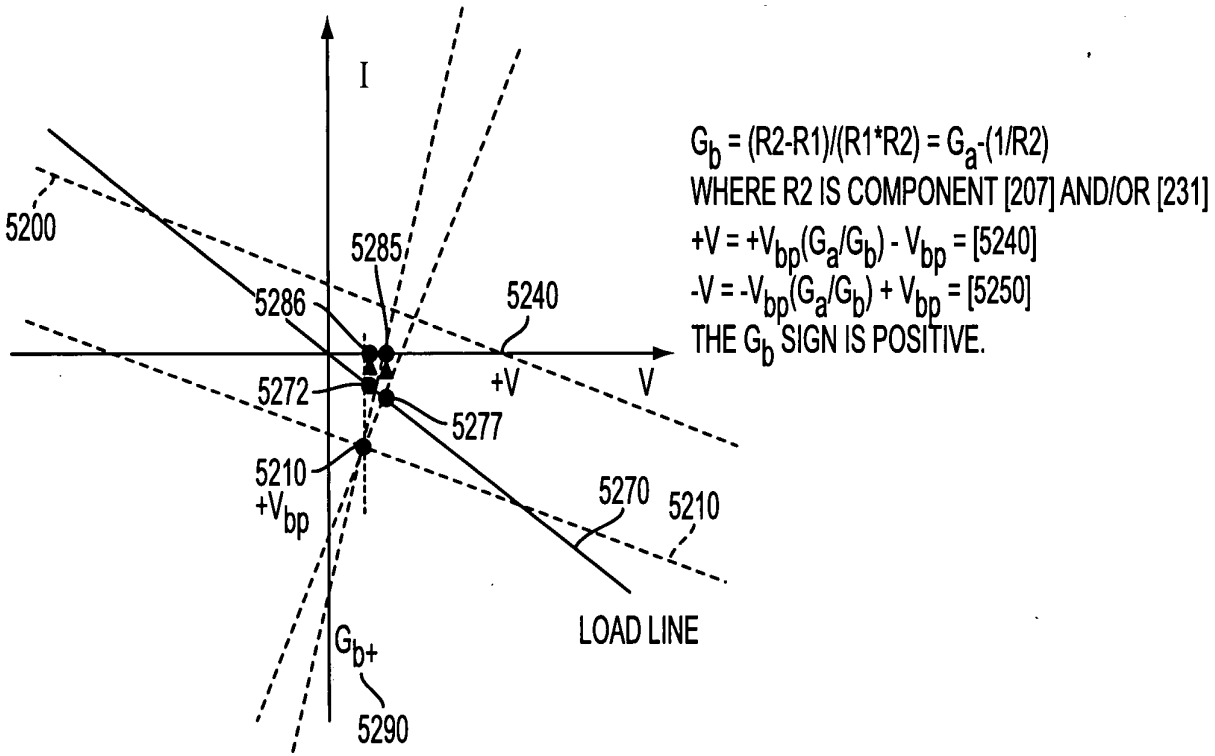
I
5200
5285
5286
5240
+V
V
5272
5277
5210
+Vbp
5270
5210
LOAD LINE
Gb+
5290
Gb = (R2-R1)/(R1*R2) = Ga-(1/R2)
WHERE R2 IS COMPONENT [207] AND/OR [231]
+V = +Vbp(Ga/Gb) - Vbp = [5240]
-V = -Vbp(Ga/Gb) + Vbp = [5250]
THE Gb SIGN IS POSITIVE.

FIG. 52